INVESTIGATIONS OF TECHNICAL PROBLEMS IN GALLIUM
ARSENIDE

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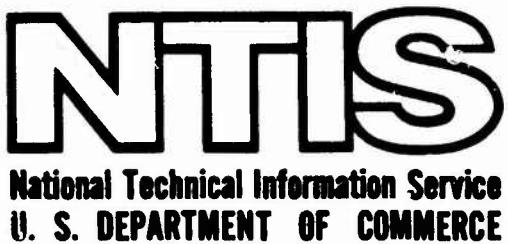
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INVESTIGATIONS OF TECHNICAL PROBLEMS IN GALLIUM ARSENIDE

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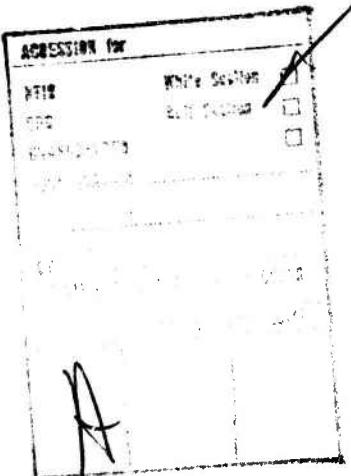
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Various technological problems in the development of GaAs microwave devices are covered in this report. The goal is to advance the state-of-the-art in material and device technology. The work reported here includes: epitaxial growth of ultra-thin and high-resistivity films, study of the relationship between device performance and material parameters using IMPATT diodes, annealing study of $n-n^+$ interfaces to improve their electrical properties, growth of semi-insulating substrates and characterization techniques, and study of ion implanta-

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tion as a tool for microwave device fabrication. The activities and the progress made during the six-month period are described in separate sections. Future plans for the next reporting period are also included. This work is being carried out in cooperation with the California Institute of Technology, Cornell University, Crystal Specialties, and Stanford University

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1.0 INTRODUCTION

The widespread application of GaAs devices in micrcwave systems is yet to be realized despite their superior performance characteristics. The lag of reproducibility and reliability in these devices has resulted in low yield and high unit cost. These drawbacks overshadow the advantages in performance, some of which are unique to GaAs devices. For instance, the high electron mobility in GaAs permits the fabrication of FET's operating at frequencies far beyond the cutoff of the bipolar transistor. The combination of high electron mobility in the low field region and the large difference in electron and hole ionization coefficients recently led to the realization of very high efficiency (> 30%) GaAs IMPATT devices. In addition, the transferred electron device, which is made possible by the negative differential mobility, is just unattainable from other better-known semiconductors such as silicon or germanium. The urgent need of improved microwave devices for high data rate communication is approaching due to the advent of the digital computer. The currently available frequency spectrum allocated for communication is nearly filled. It is certain that an improvement in GaAs technology will help to alleviate many device and system difficulties in microwave frequencies beyond X-band and perhaps well into the mm-wave frequencies.

A joint program between the Science Center and several leading universities was conceived and initiated in 1973 to investigate and solve the technological problems in the development of GaAs devices. Crystal Specialties, a leading GaAs substrate material supplier, was brought in after October, 1974, to replace the University of Southern California to provide substrates for the research program. The IMPATT diode and the Schottky barrier field effect transistor were chosen as the experimental vehicles for the studies of GaAs material and technology. The areas of research relevant to these devices are:

1. Growth and quality evaluation of semi-insulating substrates in terms of electrically-active trap densities and crystal dislocations.

2. Growth of ultra-thin epitaxial layers.

3. Formation of low resistivity ohmic contacts.

4. Formation of semi-insulating areas by proton bombardment.

5. Ion implantation to form n-type layers on insulating substrates or device structures.

6. RF measurement on GaAs devices for material characterization and technology evaluation.

The above activities are carried out at the Science Center closely coordinated with the participating universities. Improvement in reliability and yield of microwave devices is anticipated as a direct result of this GaAs technology program.

2.0   PROGRAM GOALS AND TECHNICAL APPROACH

2.1   Epitaxial Material Growth and Characterization

The goal is to investigate material and processing technology to improve the control of growth parameters, enhancing the reproducibility and the reliability of devices. Problems related to epitaxial film properties such as the uniformity in thickness and carrier concentration, dislocation density, surface damage, and background impurity densities are studied.

2.1.1   High-Resistivity GaAs Layers

This research program is aimed at establishing parameters (temperature, dopants, distribution coefficients, etc.) necessary for the growth of thin layers of high sheet resistance ($\approx 10^4$ ohm/□) GaAs on semi-insulating GaAs substrates by means of liquid phase epitaxial (LPE) techniques. In addition, the electrical properties of these layers will be measured to study their electron transport mechanisms and to provide information for device applications.

2.1.2   Material Characterization--Theoretical and Experimental Investigation of the Effect of Material Properties on Device Performance

Electrical measurements performed on GaAs devices are employed to evaluate the effect of material parameters on device performance. Basic material parameters, such as the asymmetry of the hole and the electron ionization rate, are to be derived from data obtained on GaAs IMPATT amplifiers.

2.2   Semi-Insulating Material

The goal is to prepare and to establish methods to evaluate semi-insulating GaAs crystals with the emphasis placed on the effect of deep traps in FET's

fabricated on such substrates. The roles of impurities such as O and Cr are investigated. Breakdown measurements of p-i-p, n-i-n, and n-i-m structures are employed to investigate the electrically active trap densities. The potential distribution in these structures under d-c bias is studied using high spatial resolution Auger spectroscopy.

2.3 Ion Implantation

The goal is to investigate the effect of ion beam energy, dosage, and species of impurities on the carrier concentration profile of ion-implanted GaAs substrates under various annealing conditions. The effectiveness of the annealing caps for the substrate surface during the annealing process is also being investigated. A combination of controlled stripping and C-V Hall measurements is being used to characterize the implanted layer.

3.0 RESULTS

3.1 Epitaxial Material Growth and Material Characterization

3.1.1 High-Resistivity GaAs

3.1.1.1 Growth Studies. In order to reduce the impurities produced from the chemical reactions between the components used in the growth system, a less reactive pyrolytic BN growth cell was used in place of the earlier graphite growth cell. During the past six months, 42 GaAs LPE layers have been grown in four separate series in which the same melt was maintained throughout each individual series. Tables 3.1-1, 3.1-2, 3.1-3, and 3.1-4, which list the results of each individual series separately, show

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that high quality, low free carrier density layers can be
obtained with this system. From Table 3.1-1 we can see that
the bakeout transition temperature above which the layers con-
vert to p-type in the SiO_2-BN(C)-H_2 system is in the vicinity
of 700°C, instead of 775°C as found for the earlier SiO_2-C-H_2
system.

The second growth series, detailed in Table 3.1-2, was carried
out with a new melt to see if the data of Table 3.1-1 could be
repeated. It is not unusual to find that the first or second
growth from a new melt is n-type, as it takes a certain amount
of settling time for the layers to reflect the melt bakeout
conditions. However, the fact that run #907 is n-type is cer-
tainly unexpected. This might be attributed to an accidental
contamination of the melt between runs #902 and 907 which was
"cleaned up" after a strong 49-hour bake at 750°C. Note that
runs #908 and 909 are p-type. After an 89-hour bake at 700°C
subsequent runs were n-type, again suggesting that the transi-
tion temperature is in the vicinity of 700°C.

In the third growth series, Table 3.1-3, all layers were n-type.
A 750°C bakeout for 22 hours was insufficient to drive run
#1005 p-type either because of melt contamination or insufficient
bakeout time. Likewise, runs #1010 and 1011 remained
n-type.

The effect of adding 0.5 atomic % Cr to the melt was investi-
gated in the last four runs of the third growth series. The

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Table 3.1-1 Properties of Epitaxial GaAs Layers Grown in a Pyrolytic Boron Nitride (Graphite), Fused-Quartz and Hydrogen Growth System. Growth Series 800; H_2 Flow Rate: 0.6 ℓ/min; Substrate Orientation: (100)

Growth No.	Bakeout Temp./Period (°C)/(Hr)	Saturation Temp. (°C)	Annealing Temp./Period (acc.) (°C)/(Hr)	Mobilities @ 300/77°K (cm²/v-sec)	Carrier Densities @ 300/77°K (cm⁻³)	Resistivity @ 300°K (ohm-cm)	Conductivity Type
801	700/24	700	---	6,000/31,000	$3.6 \times 10^{15}/3.0 \times 10^{15}$	0.29	n
802	700/14	700	---	----	---	--	p
			750/24	310/5,300	$2.3 \times 10^{16}/7.7 \times 10^{13}$	0.87	p
			750/48	270/5,300	$2.8 \times 10^{16}/9.0 \times 10^{13}$	0.83	p
803	700/12	700	---	----	---	--	p
804	750/24	750	---	----	---	--	p
			750/24	370/7,500	$3.8 \times 10^{15}/4.5 \times 10^{13}$	4.5	p
805	750/36	750	---	270/--	$1.2 \times 10^{15}/--$	19.6	p
			750/24	310/--	$3.3 \times 10^{15}/--$	6.1	p
806	750/24	750	---	430/9,800	$1.3 \times 10^{14}/5.2 \times 10^{13}$	107	p
807	600/36	600	---	----	---	--	n
808	600/18	750	---	8,900/88,000	$1.4 \times 10^{14}/1.3 \times 10^{14}$	5.04	n
809	600/36	750	---	8,100/76,000	$2.7 \times 10^{14}/2.5 \times 10^{14}$	2.9	n

Table 3.1-2 Properties of Epitaxial GaAs Layers Grown in a Pyrolytic Boron Nitride (Graphite), Fused-Quartz and Hydrogen Growth System. Growth Series 900; H_2 Flow Rate: 0.6 ℓ/min Substrate Orientation: (100)

Growth No.	Bakeout Temp./ Period (°C)/(Hr)	Saturation Temp. (°C)	Mobilities @ 300/77°K (cm^2/v-sec)	Carrier Densities @ 300/77°K (cm^{-3})	Resistivity @ 300°K (ohm-cm)	Conductivity Type
901	750/19	750	6,900/55,000	$6.8\times10^{14}/5.8\times10^{14}$	1.3	n
902	750/24	750	7,900/88,000	$7.5\times10^{13}/4.2\times10^{13}$	11	n
907	750/25	750	8,300/56,000	$3.7\times10^{14}/3.3\times10^{14}$	2.0	n
908	750/49	750	280/--	$8.2\times10^{14}/--$	27	p
909	775/60	750	470/6,700	$3.1\times10^{14}/2.5\times10^{14}$	43	p
910	700/89	700	7,100/48,000	$8.9\times10^{14}/8.5\times10^{14}$	0.98	n
912	700/24	700	8,300/63,000	$2.8\times10^{14}/2.5\times10^{14}$	2.7	n

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Table 3.1-3 Properties of Epitaxial GaAs Layers Grown in a Pyrolytic Boron Nitride (Graphite), Fused-Quartz and Hydrogen Growth System. Growth Series 1000; H_2 Flow Rate: 0.6 ℓ/min Substrate Orientation: (100)

Growth No.	Dopant	Bakeout Temp./Period (°C)/(Hr)	Growth Temp./Cooling Rate (°C)/(°C min^{-1})	Mobilities @ 300/77°K (cm²/v-sec)	Carrier Densities @ 300/77°K (cm^{-3})	Resistivity @ 300°K (ohm-cm)	Conductivity Type
1001	--	750/15	700/12.5	7,000/65,000	$8.1\times10^{14}/6.9\times10^{14}$	1.1	n
1002	--	650/15	650/12.0	8,100/36,000	$3.5\times10^{15}/3.0\times10^{15}$	0.22	n
1003	--	650/17	650/12.0	7,000/52,000	$6.5\times10^{14}/6.1\times10^{14}$	1.4	n
1004	--	650/16	650/12.0	7,700/50,000	$1.7\times10^{15}/1.5\times10^{15}$	0.48	n
1005	--	750/22	700/12.5	7,700/62,000	$9.1\times10^{14}/7.9\times10^{14}$	0.9	n
1006	--	650/18	650/12.0	6,800/57,000	$9.8\times10^{14}/8.4\times10^{14}$	0.94	n
1007	--	700/16	700/13.0	8,900/67,000	$8.0\times10^{14}/8.0\times10^{14}$	0.88	n
1008	--	700/12	700/13.0	8,500/80,000	$5.5\times10^{14}/5.2\times10^{14}$	1.4	n
1009	--	700/18	700/13.0	8,400/--	$5.7\times10^{14}/--$	1.3	n
1010	--	730/21	730/0.9	9,000/103,000	$2.5\times10^{14}/8.4\times10^{14}$	2.8	n
1011	--	730/19	700/13.0	8,500/86,000	$3.7\times10^{14}/3.9\times10^{14}$	2.0	n
1012	Cr (0.5 atm %)	730/12	700/13.0	7,200/44,000	$2.0\times10^{15}/1.8\times10^{15}$	0.43	n
1013	Cr (0.5 atm %)	750/15	700/4.5	6,900/75,000	$3.4\times10^{14}/3.2\times10^{14}$	2.7	n
1014	Cr (0.5 atm %)	750/13	700/4.5	6,200/56,000	$1.7\times10^{14}/1.4\times10^{14}$	6.1	n
1015	Cr (0.5 atm %)	750/13	700/4.5	8,100/86,000	$1.6\times10^{14}/1.8\times10^{14}$	4.8	n

first layer (#1012) grown from the Cr-doped melt had a high

carrier density, but in subsequent runs (#1013-1015) the densi-

ties decreased rapidly and leveled off in the low 10^{14} cm^{-3}

range. This might suggest that there are some unknown impuri-

ties with large segregation coefficients (> 1) in the Cr

source.

Several runs in the third growth series (#1010, 1011, 1015)

show larger carrier concentrations at 77°K than at 300°K. Layers

occasionally exhibit high Van der Pauw correction factors indi-

cating poor ohmic contacts, which are often difficult to maintain

at liquid nitrogen temperatures. This effect may be the cause of

the anomalies in carrier density.

In the 1100 series of growths, Table 3.1-4, the Ga in the cradle

was eliminated in order to reduce direct contact between Ga and

graphite. Note that the growth system in this series is

SiO_2-BN(C)-H_2. For each layer grown from this melt, the bakeout

temperature was maintained at 600°C for a period of approximately

16 hours and the saturation temperature was fixed at 700°C. An

electronic ramp generator was used to maintain a constant cooling

rate of 4.5°C/min during growth. Under these conditions, the

carrier density increases with accumulated bakeout time as shown

by Curve (B) in Fig. 3.1-1. Curve (A) in Fig. 3.1-1 shows that

the carrier density of layers grown from the earlier SiO_2-C-H_2

system decreases with accumulated bakeout time. One possible

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Table 3.1-4 Properties of Epitaxial GaAs Layers Grown in a SiO_2-BN(C)-H_2 (without Ga in Graphite) Growth System. Growth Series 1100

Growth Conditions: Initial Bakeout @ 850°C, 2 hrs.
H_2 Flow Rate: 0.6 ℓ/min
Bakeout Temp: 600°C; Bakeout Period: ~ 16 hrs.
Saturation Temp: 700°C; Cooling Rate: 4.5°C/min.
Substrate Orientation: (100)

Growth No.	Mobilities @ 300/77°K (cm^2/v-sec)	Carrier Densities @ 300/77°K (cm^{-3})	Resistivity @ 300°K (ohm-cm)	Conductivity Type
1101	8,800/110,000	$1.8/1.6 \times 10^{14}$	3.9	n
1102	8,600/91,000	$2.8/2.9 \times 10^{14}$	2.6	n
1103	5,500/77,000	$4.6/4.3 \times 10^{14}$	2.5	n
1104	8,400/79,000	$6.0/5.4 \times 10^{14}$	1.3	n
1105	8,500/87,000	$3.9/3.7 \times 10^{14}$	1.9	n
1106	9,200/71,000	$8.8/8.5 \times 10^{14}$	0.77	n
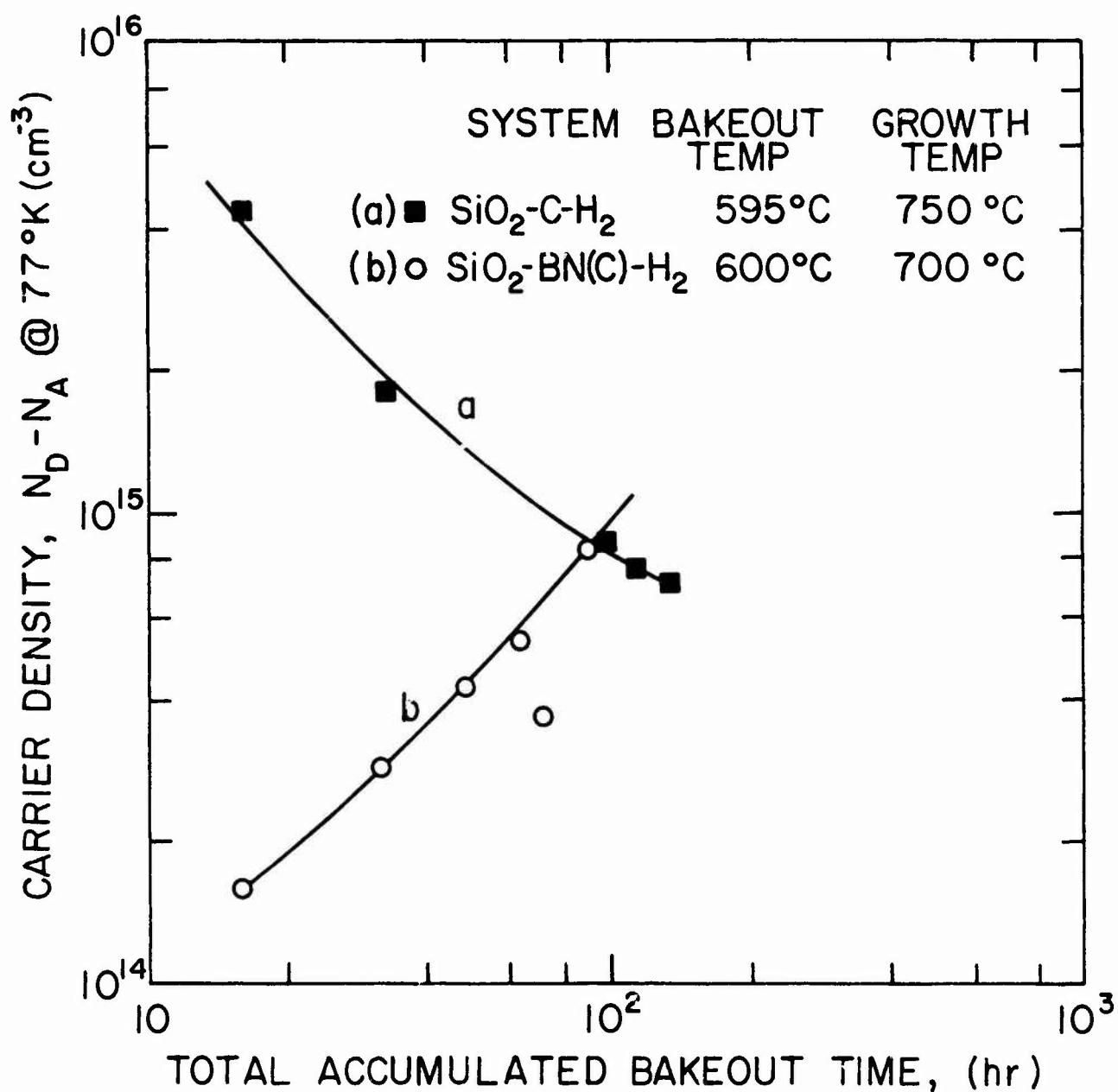
Fig. 3.1-1 Carrier density vs accumulated bakeout time for
SiO$_2$-CH$_2$ and SiO$_2$-BN(C)-H$_2$ systems.

reason for the different results in these two experiments is the type and/or density of impurities, such as carbon, in the melts. Further studies of this difference will be carried out by replacing the graphite cradle with a fused quartz cradle when using the BN cell.

3.1.1.2 Photoluminescence Studies. Photoluminescence measurements, using a 4W argon ion laser as the excitation source, were carried out in an attempt to identify the various impurities and defects in our grown layers. Table 3.1-5 lists the energy levels of selected impurities and complexes in GaAs as obtained from the literature. A comparison of these energy values with our recorded photoluminescence spectra are used for identification purposes.

The photoluminescent spectrum from n-type layer #809, grown from an undoped melt baked out at 600°C, is given by Curve (A) of Fig. 3.1-2 and shows a broad peak approximately 6 meV below the band-to-band transition energy (B-B). It is reasonable to assume that this peak involves transitions between the valence band and either Si on Ga sites (Si_{Ga}) or C on Ga sites (C_{Ga}). The peak intensity from p-type layer #806, grown from the same melt after bakeout at 750°C, has a maximum at approximately 22 meV below the B-B energy, as shown in Curve (B) of Fig. 3.1-2. This peak may involve transitions between C on As sites (C_{As}) or Si on As sites (Si_{As}), both of which are acceptors, to shallow donor levels or to the conduction band.

Table 3.1-5   Ionization Energies in GaAs

Species	Type	Level (eV)	Reference
Band Gap	B-B	1.512	(a)
Si_{Ga}	Donor	0.00581	(b)
C_{Ga}	Donor	0.006	(c)
O_{As}	Donor	0.75	(d)
Cu	Acceptor	0.15	(e)
C_{As}	Acceptor	0.019	(f)
Si_{As}	Acceptor	0.030	(g)
Cr	Acceptor	0.79	(h)
Si_{As}-Si_{Ga} or Si_{Ga}-V_{Ga}	Acceptor	0.10	(i)

References to Table 3.1-5

(a)   E. W. Williams and H. B. Bebb, Semiconductors and Semimetals, Vol. 8, R. K. Willardson and A. C. Beer, editors (Academic Press, New York, 1972), p. 321.

(b)   C. J. Summers, R. Dingle, and D. E. Hill, Phys. Rev. B1, 1603 (1970).

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(e)   F. D. Rose, D. Meyerhofer, and R. V. Jensen, J. Appl. Phys. 31, 1105 (1960).

(f)   S. M. Sze and J. C. Irvin, Solid-State Electron. 11, 599 (1968).

(g)   E. W. Williams, Solid State Comm. 7, 541 (1969).

(h)   R. W. Haisty and G. R. Cronin, Proc. of 7th Int. Conf. on the Phys. of Semiconductors, Paris, 1964 (Dunod, Paris, 1964), p. 1161.

(i)   W. G. Spitzer and W. Allred, J. Appl. Phys. 39, 4999 (1968).
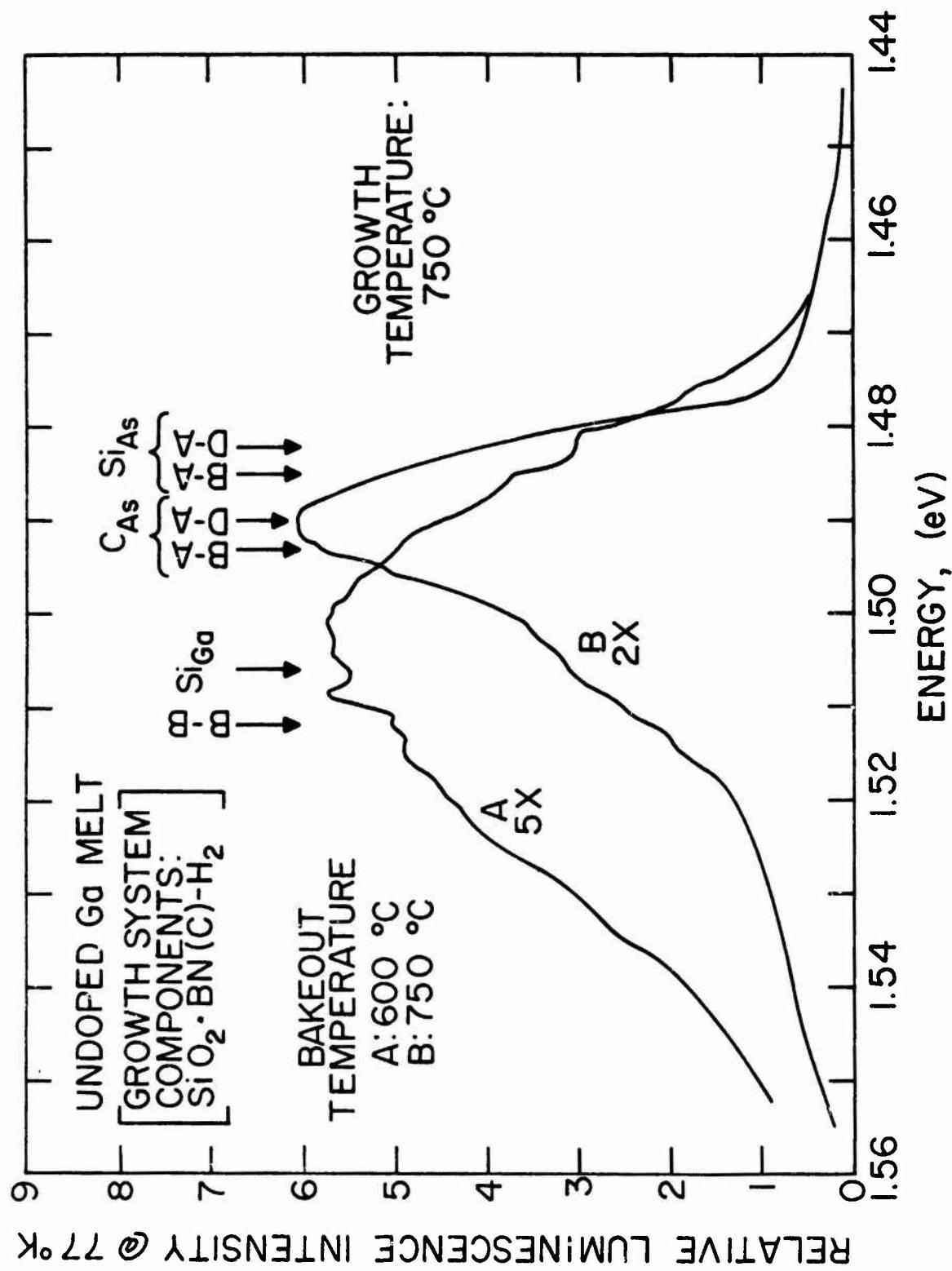
Fig. 3.1-2 Photoluminescence spectra of LPE GaAs layers grown in a SiO_2-BN(C)-H_2 growth system. Curve A for n-type layer #809. Curve B for p-type layer #806.

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Although both layers were grown at 750°C, the melt was baked
out at 600°C for one and 750°C for the other. We believe that
the bakeout tends to free or tie up impurities in the melt so
that they enter the crystal in different proportions according
to the bakeout temperature. The photoluminescence results
lead to the conclusion that n-type material results when Si or
C substitute on Ga sites, while p-type material results when
either of these reside on As sites. However, it is not possible
to assign definite site locations from this data alone.

Rosztoczy[1] has reported that the doping nature of Si depends on
its concentration in the melt, resulting in n-type material for
low Si concentrations. This leads one to the conclusion that
the donor species in our layers is Si_{Ga}, presuming that the Si
concentration in the melt decreases at lower bakeout tempe
However, Hicks and Green[2] have reported obtaining p-type mate
for all Si melt concentrations. These discrepancies may be due
to different growth system components, preparation (bakeout) and
growth conditions which were not reported. On the other hand,
the fact that the transition temperature in our experiments is
lowered for the system involving a BN liner (resulting in less
available C) leads one to suspect that C_{Ga} may be responsible for
n-type behavior while Si_{As} may be responsible for p-type behavior.
At this time, no definite conclusions can be made and further

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study is required. Elimination of C from the growth system
should give additional insight into the problem.

3.1.1.3 Annealing of LPE GaAs. We have found that it is diffi-
cult to make good ohmic contacts to some layers grown from melts
baked in the transition temperature range of $\approx 700°C$ in the
SiO_2-BN(C)-H_2 system. However, better ohmic contacts were
achieved after annealing these layers at 750°C in a H_2 flow.
All of these layers become more p-type after the annealing, Table
3.1-1. From carrier density versus 1/T data, obtained from
Van der Pauw measurements on sample #802, an activation energy of
94 meV was found (Fig. 3.1-3). A possible mechanism involved in
the heat treatment is the in-diffusion of As vacancies (V_{As})
from the surface to which Si atoms, already present in the layer,
diffuse to form Si_{As} centers. Thus, the 94 meV activation energy
may be associated with energy levels formed by either $(Si_{As}-V_{As})$
or $(Si_{As}-Si_{Ga})$ complexes (see Table 3.1-5).

3.1.2 Material Characterization

3.1.2.1 Computer-Aided Diode Analysis. It has been common prac-
tice in recent publications concerning avalanche diodes to simply
plot the susceptance vs the conductance as a function of exper-
mental parameters such as the frequency, bias current, or r.f.
amplitude. A typical plot is shown in Fig. 3.1-4 where the full
lines represent constant current and r.f. amplitude, while the
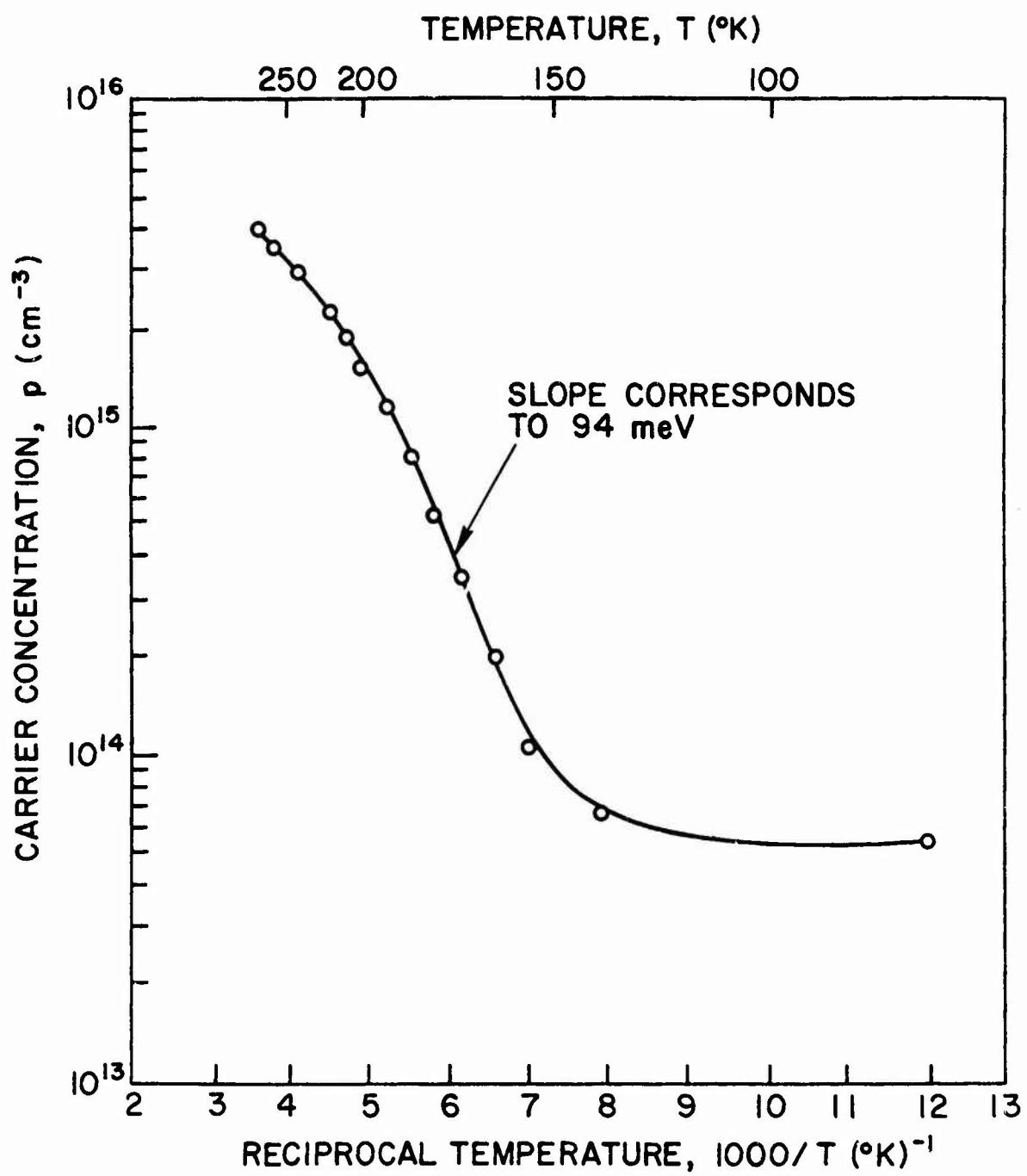
Fig. 3.1-3 Carrier concentration obtained from Van der Pauw
measurements as a function of reciprocal temperature.
Sample 802 after annealing at 750°C for 48 hrs.
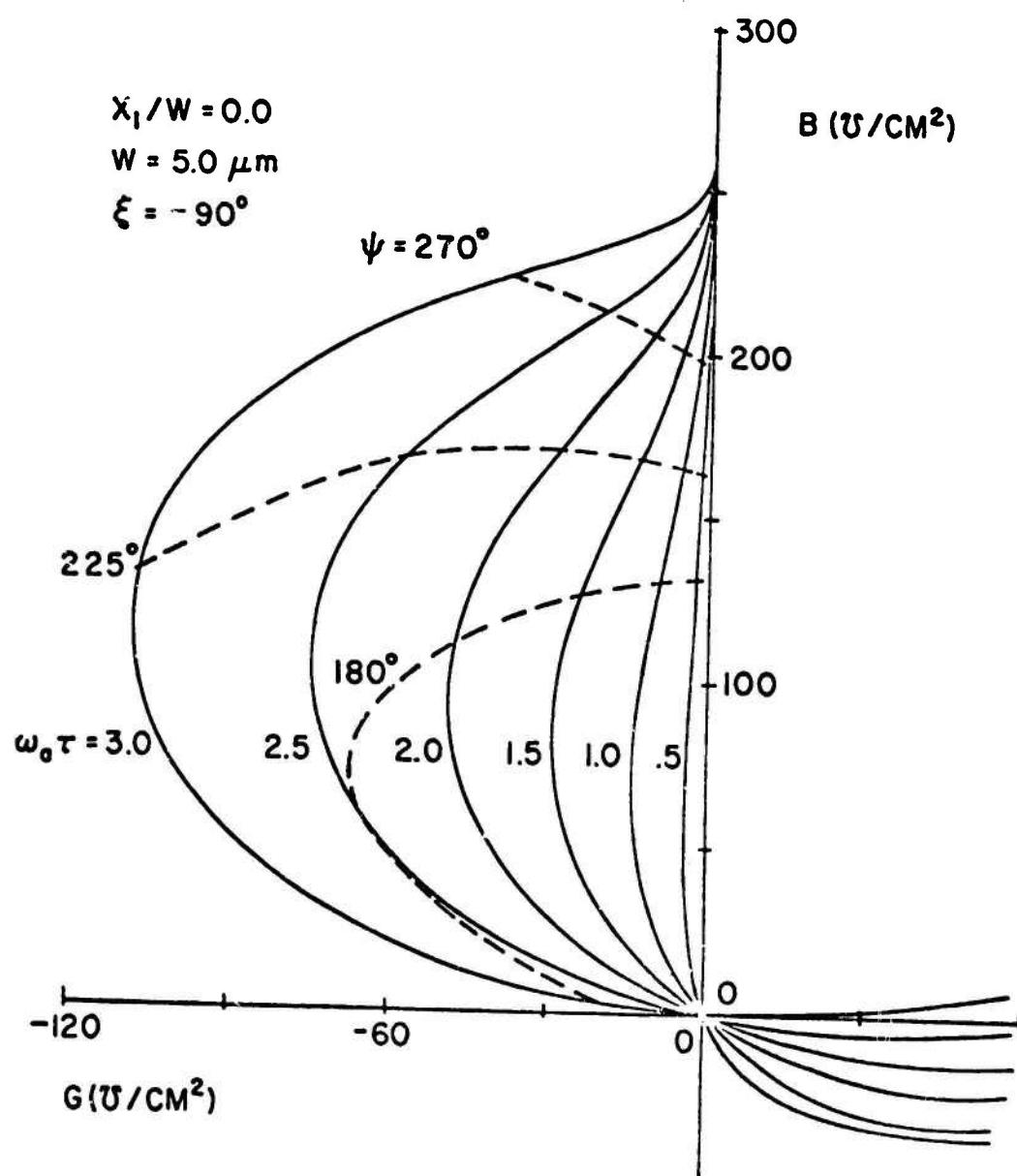
Fig. 3.1-4 Conventional plot of avalanche diode admittance showing constant current and constant frequency contours.

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dotted lines represent constant frequency contours. It is quite
difficult to determine by inspection a favorable operating region
or even whether a given set of amplifier specifications can be
satisfied by a diode whose admittance is plotted in this
fashion.

From our studies of the nonlinear diode-circuit interaction it
has become apparent that the single most important diode
parameter is the electronic quality factor, Q_{po} (for a more
detailed discussion, see Sec. 3.1.2.2). For example, an ampli-
fier specification of operating gain and minimum distortion
requires $Q_{po} < Q_{po\ max}$. Since Q_{po} is defined as the ratio of
the diode electronic susceptance to conductance, it would seem
appropriate to plot these components rather than those of the
total diode admittance. Accordingly, the diode transition
susceptance has been subtracted from the total susceptance leav-
ing only the electronic part which was then normalized to the
transition susceptance at the design point avalanche resonance
frequency, ω'_a. The resulting plot of electronic diode admittance
is shown in Fig. 3.1-5. The circles and pluses represent a Read
structure with an avalanche zone that is 10% of the transition
width while the squares and crosses represent the admittance
behavior of an n-Si IMPATT with a uniformly-doped active region.
The much greater flexibility of amplifier design using the Read
structure is immediately apparent from the lower operating values
of Q_p. This same point is again emphasized by the normalized

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Design Point Data: $\beta = .1$ at $\psi = \pi$, $\omega_a' = \pi v/(w-x_1)\sqrt{10}$

$G_d/\omega_a'C_o$

-1.5   -1.0   -.5   0

$Q_p < .5$

$\beta = .3$

$> .5$

< 1.0

> 1.0

< 2.0

> 2.0

.1
.2
.4
.5
.6
.7

.1
.2
.3
.4
.5
.6
.7
.8
.9

X.2
X.3
X.4

.2
.3
.4

$B_e/\omega_a'C_o$

-.5
-1.0
-1.5
-2.0

—⊙— Constant frequency
$\psi = \pi$, $x_1/w = .1$
—+— Varying frequency
—□— Constant frequency
$\psi = \pi$, $x_1/w = .4$
—×— Varying frequency
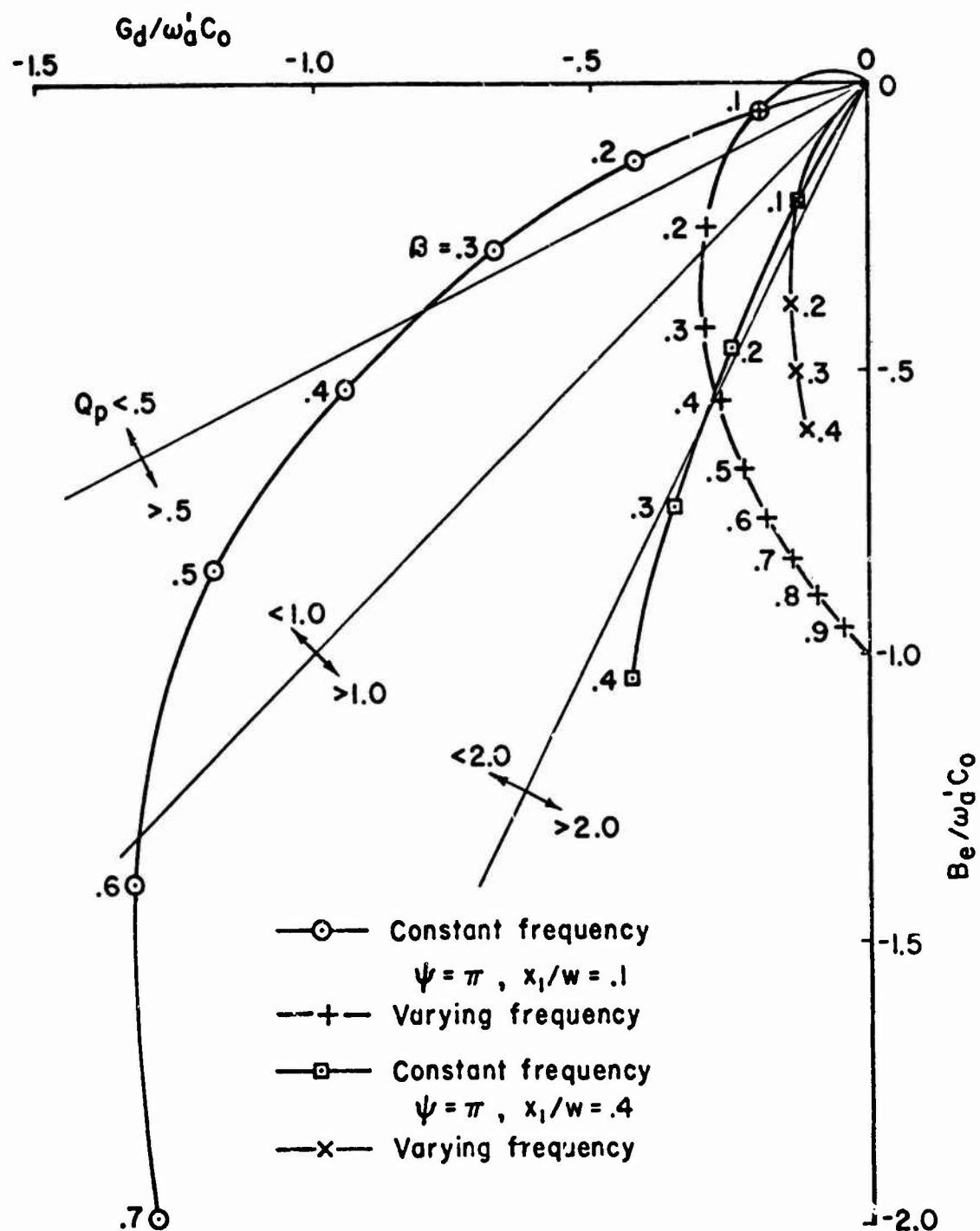
Fig. 3.1-5 Plot of the electronic components of the avalanche diode
admittance showing constant frequency and constant
current-r.f. amplitude contours of .1W and .4W.

20

curves of Fig. 3.1-6 showing the effect of varying Q_p for a simple
tuned amplifier. A rather strong precedence for the choice of
variables shown in Fig. 3.1-5 can be found in the old klystron
literature where it was utilized in a similar context.

3.1.2.2 Evaluation of the Effective Avalanche Zone Width and
         Electric Field Dependence of the Ionization Rates. In
earlier reports[3] we presented data on the variation in the gain
and frequency of an amplifier as a function of bias current and
of incident power. From this gain and frequency data the
normalized diode conductance and susceptance may be extracted
and when the circuit parameters are known the diode admittance
may be calculated.

An important property of the diode is the electronic quality
factor

$$Q_{po} \equiv \text{(electronic reactance)/(negative resistance)}$$

$$Q_{po} = \frac{\sin\psi + \psi x_1/(w-x_1)}{1 - \cos\psi} \quad .$$

(1)

This factor is dependent only on the transit angle and the rela-
tive width of the avalanche region to the drift region.

From the small signal gain vs frequency curves of an amplifier
as a function of the bias current or the incident power, the data

21
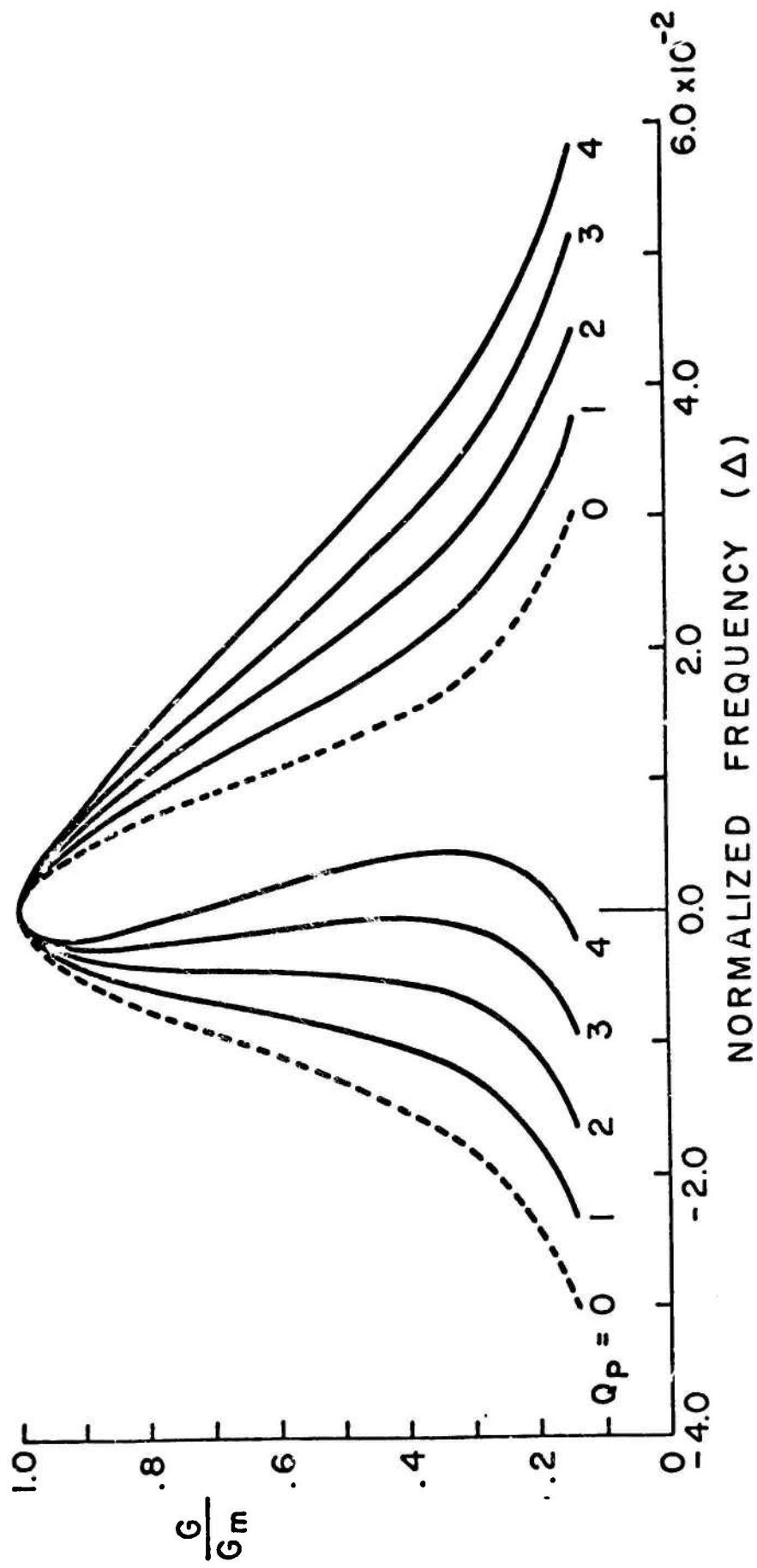
Fig. 3.1-6 Amplifier distortion as a function of the electronic quality factor Q_p.

22

shown in Fig. 3.1-7 was extracted. From this data, Q_{po} may be calculated for the current perturbation

$$Q_{po} = \frac{Q_x \frac{2\omega}{\omega_o^2} \frac{d\omega}{dI}}{d|Q_x/Q_a|/dI} \quad , \tag{2}$$

and for the power perturbation

$$Q_{po} = \frac{Q_x (2/\omega_o)[d\omega/d(\Delta p)]}{d[Q_x/Q_a]/d(\Delta p)} \quad , \tag{3}$$

and for both of these expressions $B \ll 1$ and $Q_d \gg 1$.
It can be readily seen that the data of Fig. 3.1-7 gives $Q_{po} > 0$ for Eq. (2) and $Q_{po} < 0$ for Eq. (3). The power perturbation data had been taken in a multi-slug circuit which was suspected not to reduce to a simple parallel equivalent circuit. The new circuit, which was designed and tested for the property that it does reduce to a simple parallel equivalent circuit, was used to take the data shown in Fig. 3.1-8. This new data shows a downward tuning with increased incident power and a Q_p which is inconsistent with the Q_p derived from the current perturbation data of Fig. 3.1-7.
At the peak of the gain curve the susceptance of the circuit is zero,
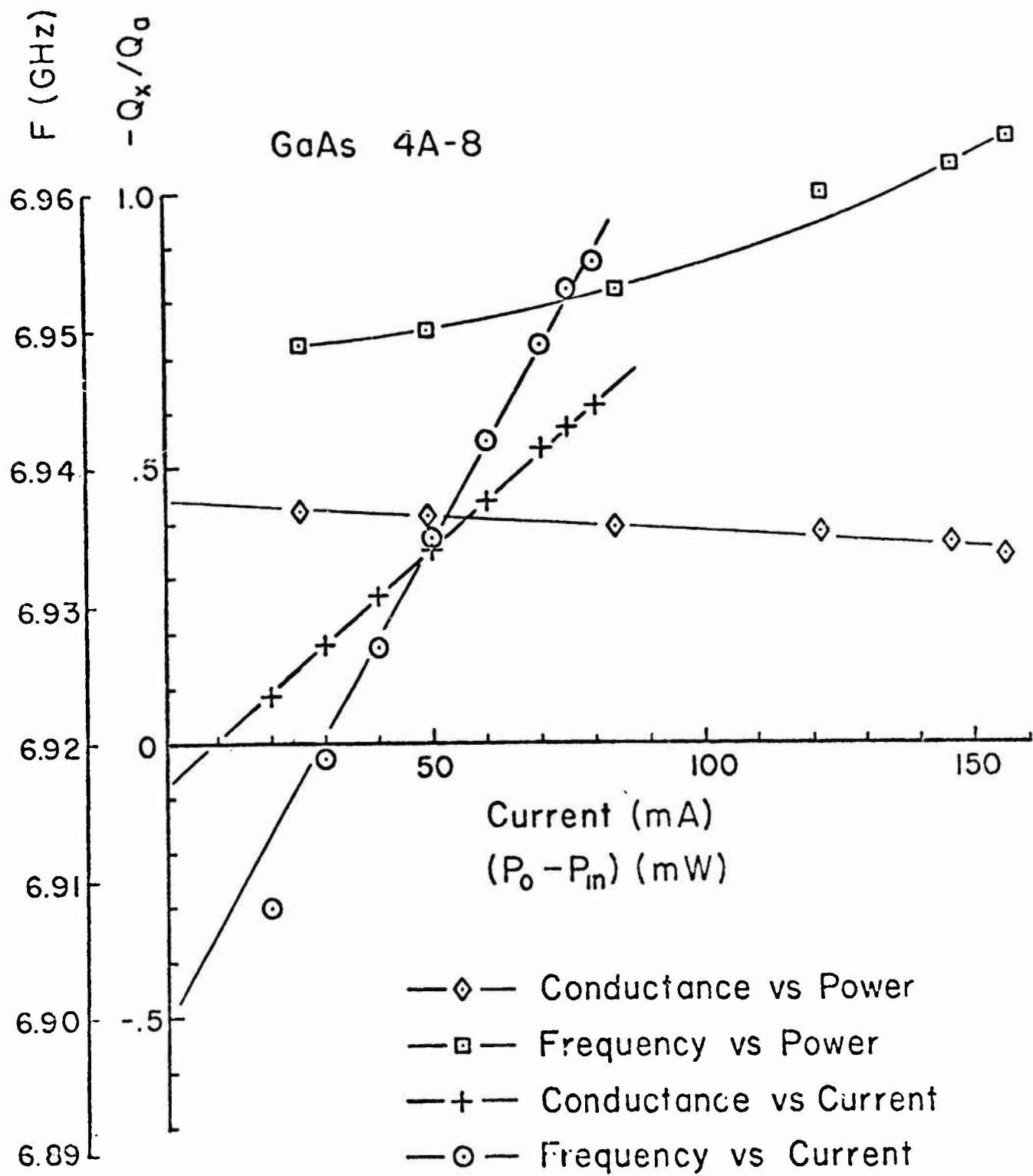
Fig. 3.1-7 Normalized amplifier conductance and frequency tuning as a function of bias current and power level for an "N" GaAs IMPATT diode.

24
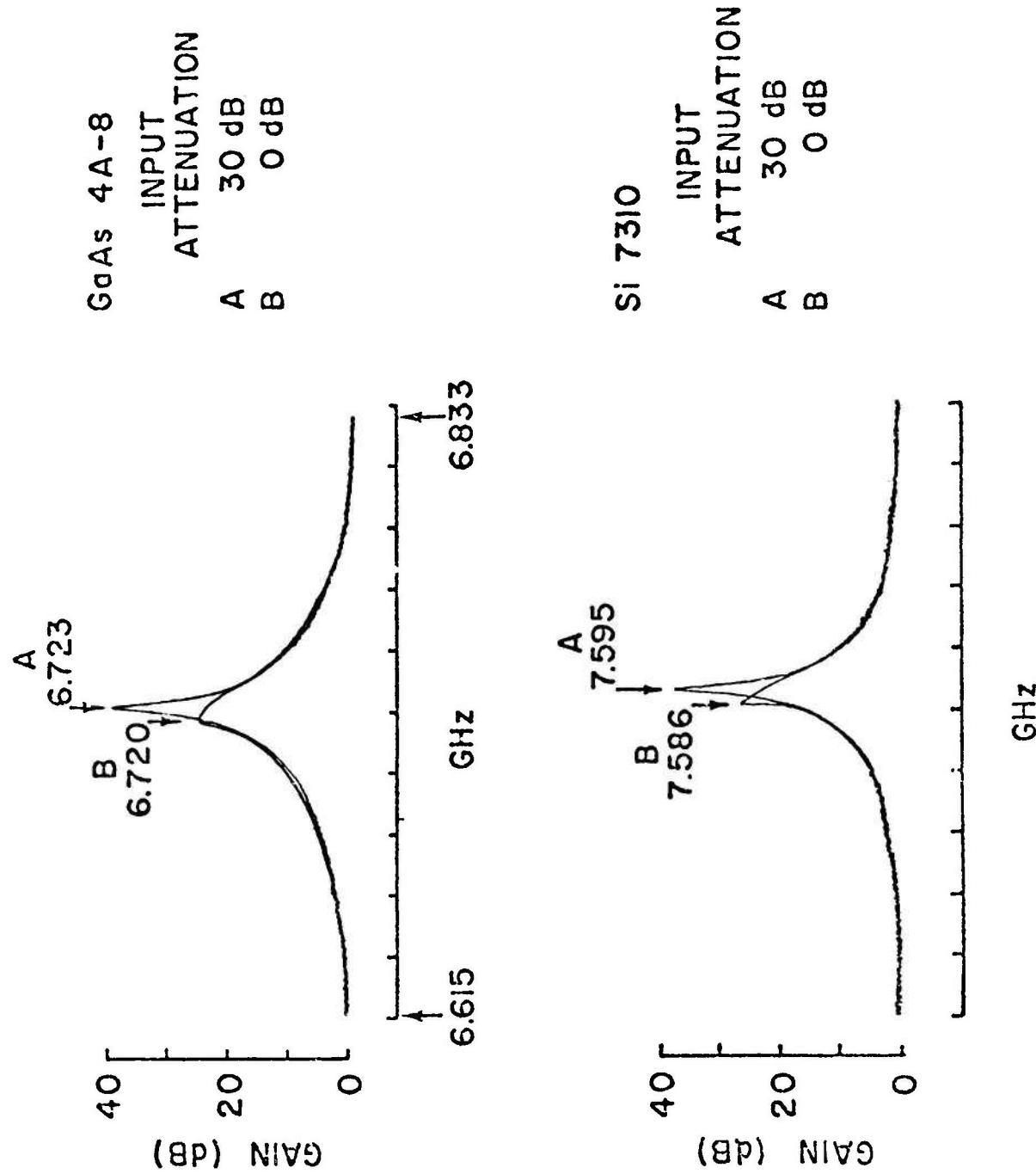
Fig. 3.1-8   Amplifier gain and frequency as a function of incident power level as observed on an H-P Network Analyzer.

$$b = Q_x(2\delta + Q_p/Q_a) = 0 \quad . \tag{4}$$

Note that $Q_p > Q_{po}$ by the factor $r_e/(r_e + r_s + r_c)$ where r_s is the series resistance due to the diode contacts and substrate, and r_c is the equivalent series resistance due to circuit losses. From Eq. (4) one can derive an expression for Q_{po} in the limit that $\delta << 1$ and $Q_x >> 1$

$$Q_{po} \simeq \frac{(f_{ss} + f_m)\Delta f}{f_0^2} \frac{Q_x}{|Q_x/Q_{ass}| - |Q_x/Q_{am}|} \quad , \tag{5}$$

where f_{ss} is the frequency of the small signal resonance, f_m the frequency of the large signal curve, and Q_x/Q_{ass} and Q_x/Q_{am} are the normalized conductance for the small and large signal cases, respectively. Note that in Eq. (5) the parasitic conductances cancel out. The value of Q_{po} obtained from several measurements of the kind shown in Fig. 3.1-8 is

$$Q_{po} = 1.0 \pm .2 \ (f = 6.72 \text{ GHz}) \quad . \tag{6}$$

Comparing this result to that obtained from the current perturbation which was

$$Q_{po} = 1.1 \pm .1 \ (f = 6.93 \text{ GHz}) \quad , \tag{7}$$

we find substantial agreement although the increasing temperature
of the junction with bias current should give higher than normal
value of Q_{po}. The present accuracy of the measurements, however,
does not permit any quantitative evaluation of such an
effect.

Having measured a value of Q_{po} close to unity, the questions
remaining to be answered are what value of x_1/w can be derived
from it and what information can be deduced about the ionization
rates? To attack these questions let us rewrite Eq. (1)

$$Q_{po} = \frac{\sin(\omega w/v_s)(1-x_1/w) + (\omega w/v_s)(x_1/w)}{1 - \cos[(\omega w/v_s)(1-x_1/w)]} \quad . \tag{8}$$

From capacity measurements on the diode, the transition width is
$w = 3.5\mu m$. Next comes the choice of the saturated velocity v_s.
Here we have used the measurements of Salmer, et al.[4] and assumed
a junction temperature less than 400°K. For this upper temperature
limit (see Fig. 3.1-9)

$$v_s(400°K) = 7.3 \times 10^6 \text{ cm/sec.} \tag{9}$$

It can be seen from Eq. (8) that a higher velocity would give
lower values of Q_{po}. Thus the value of x_1/w to be derived from
Eq. (8) will be an upper limit. Figure 3.1-10 shows a plot of Eq.
(8) using the above values for w, v_s, and a frequency of 6.72 GHz.

27
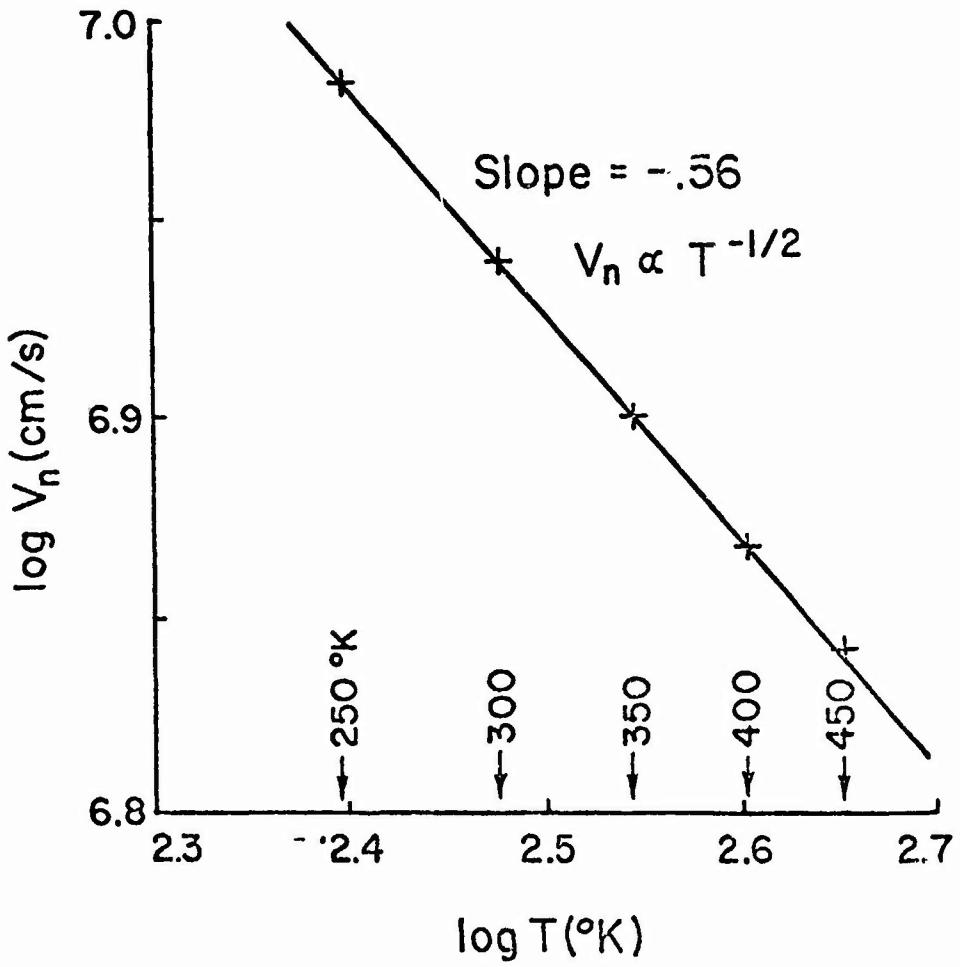
Fig. 3.1-9 Scattering-limited velocity of electrons in GaAs as a function of temperature (data replotted from G. Salmer, J. Pribetich, A. Farraye, and B. Kramer, "Theoretical and Experimemtal Study of GaAs IMPATT Oscillator Efficiency").[2]

$$V_s = 7.3 \times 10^6 \text{ cm/s}$$
$$f = 6.72 \text{ GHz}$$
$$w = 3.5 \ \mu\text{m}$$
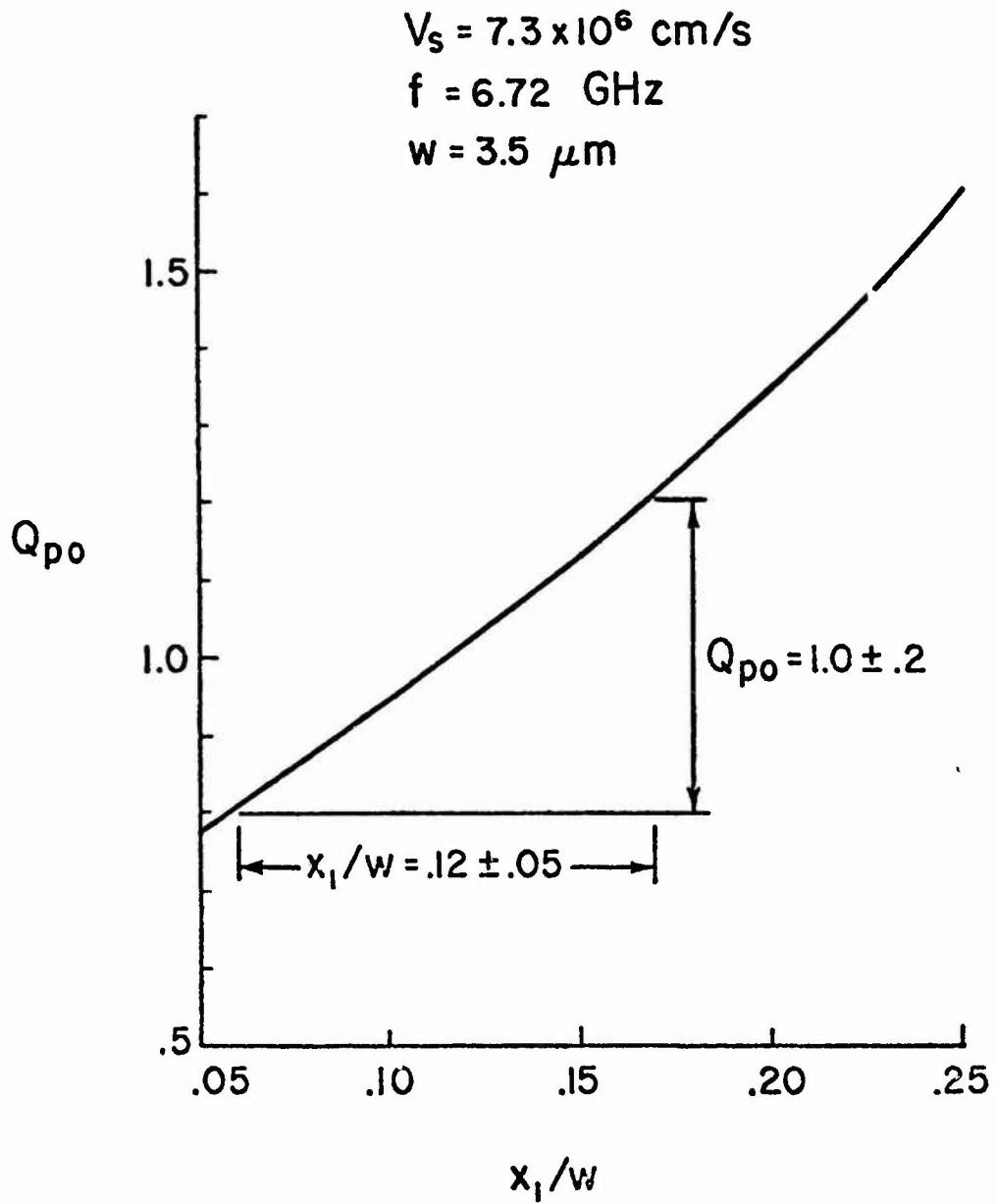
Fig. 3.1-10   Electronic quality factor as a function of the relative width of the avalanche zone for a GaAs "N" IMPATT diode.

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Taking a range of Q_{po} from 1.2 to .8, we find the corresponding
avalanche width to be

$$.06 < (x_1/w) < .17 \quad , \tag{10}$$

with a most probable value of $(x_1/w) = .12$.

The above values of (x_1/w) in GaAs for a uniformly doped active
layer are very small indeed when compared to those in Si. For
example, a comparable n-Si diode has $(x_1/w) = .4$ while a p-Si
diode has $(x_1/w) = .26$. These values of the effective avalanche
width in silicon correspond to taking a point away from the field
maximum where the ionization rate is $\sim 5\%$ of the peak value.
Quantitatively we find (x_1/w) by evaluating the equation

$$\frac{\alpha(\mathcal{E}_m)}{\alpha(\mathcal{E})} = 22 = \exp\left[\frac{b}{\mathcal{E}_m}\left(\frac{\mathcal{E}_m}{\mathcal{E}} - 1\right)\right] = \exp\left[\frac{b}{\mathcal{E}_m} \cdot \frac{x_1/w}{1 - x_1/w}\right] \quad . \tag{11}$$

In the case of GaAs where the ionizations vary with the reciprocal
of the field squared one has

$$\frac{\alpha(\mathcal{E}_m)}{\alpha(\mathcal{E})} = 22 = \exp\left\{\frac{b^2}{\mathcal{E}_m^2}\left[\left(\frac{1}{1 - x_1/w}\right)^2 - 1\right]\right\} \quad . \tag{12}$$

The peak field of diode 4A-8 at breakdown was calculated from

$$\mathcal{E}_m = 2V_B/w_B = 4.1 \times 10^5 \text{ V/cm} \quad , \tag{13}$$

using a breakdown voltage of 72 volts.

The ionization rate data of Stillman, et al.[5] has a $1/\mathscr{E}$

dependence so using Eq. (11) one obtains

$$(x_1/w) = .36 \quad \text{(Stillman, et al.)} \tag{14}$$

The data of Salmer, et al.[4] has a $1/\mathscr{E}^2$ dependence so using

Eq. (12) one obtains

$$(x_1/w) = .39 \quad \text{(Salmer, et al.)} \tag{15}$$

Using the data of McCarthy[6]

$$(x_1/w) = .31 \quad . \tag{16}$$

Thus there are no published ionization rates which would agree

with the effective avalanche width of $(x_1/w) = .12 \pm .05$

measured at microwave frequencies. Since the silicon ionization

rates a in agreement with the microwave measurements, there is

good reason for re-examining the ionization rate measurements in

GaAs.

3.1.2.3 <u>Experimental Analysis of a GaAs Read Structure</u>. Further

information about ionization rates can be gained by studying Read

structures in that the avalanche region in this case is defined

by the doping profile. This avalanche width can be determined

from capacitance and area measurements. If the avalanche width

is determined, then one can examine the effect of the non-

punch-through character on Q_p.

Figure 3.1-11 shows a set of amplifier curves on a Lo-Hi-Lo

Read diode manufactured by Raytheon. The normalized conductance

and frequency-current tuning are plotted in Fig. 3.1-12 and a

Q_p = 1.8 ± .1 is obtained from a ratio of the slopes. Next, in

Fig. 3.1-13 is shown the capacitance variation with reverse bias.

Here the first difficulty is encountered--excessive generaticn

occurs just as the space charge boundary crosses the thin, highly-

doped layer defining the end of the avalanche region. The dotted

continuation of the capacity curve is derived by imposing a break-

down condition. At the observed breakdown voltage of 24.9 volts

one can calculate a breakdown field in the narrow avalanche region

of 5×10^5 V/cm from published ionization rates. This breakdown

field implies the total number of impurities uncovered at break-

down is approximately $3.4\times10^{12}/cm^2$. Thus the doping in the two

"Lo" regions if uniform is found to be $3.4\times10^{15}/cm^3$. The electric

field profile and the impurity distribution deduced from the

capacitance measurements are shown in Figs. 3.1-14 and 3.1-15,

respectively.

The electronic quality factor may now be calculated for an

operating potential of 30V for a frequency corresponding to the

32
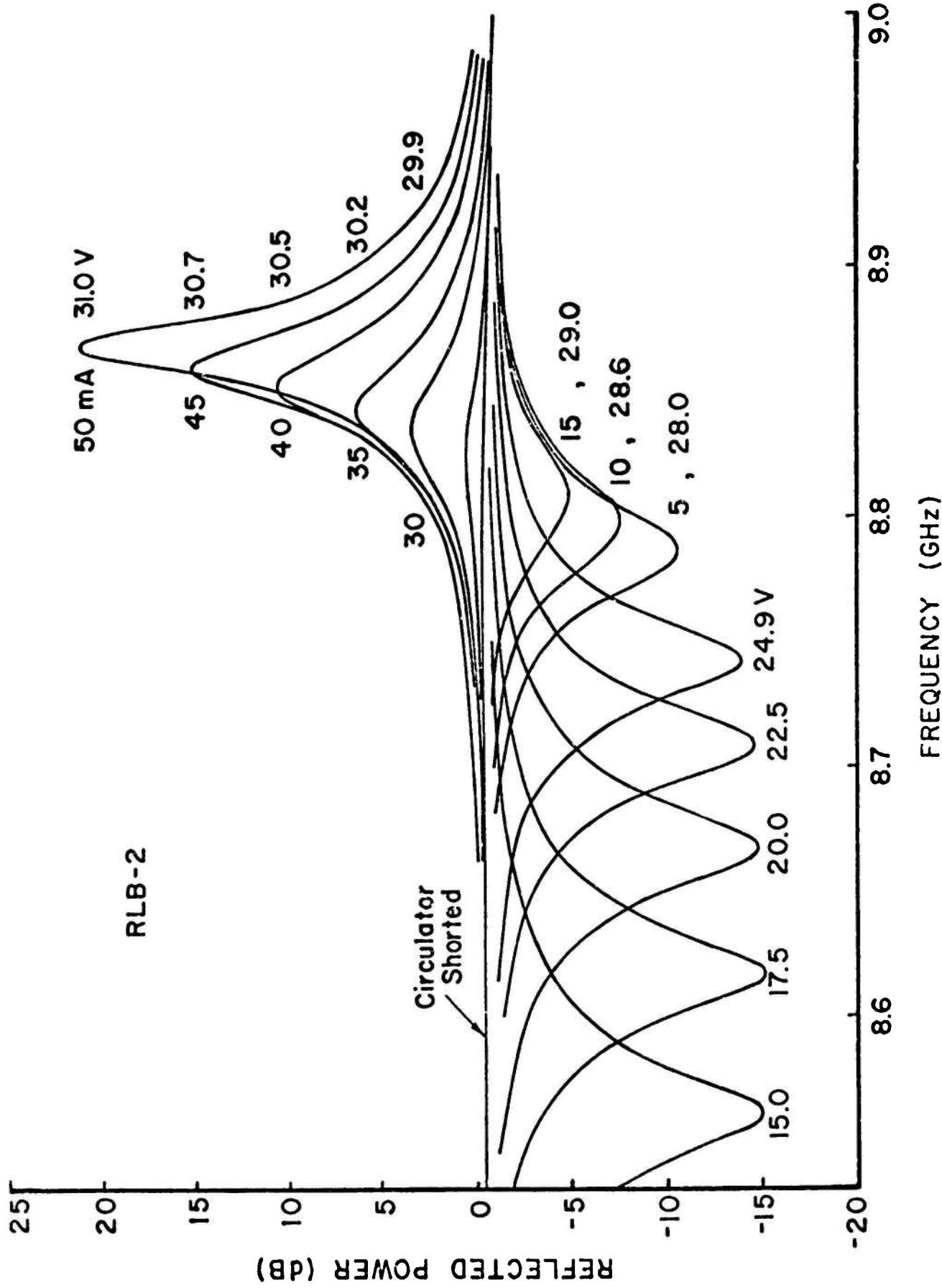
Fig. 3.1-11 Amplifier frequency response vs bias current of a GaAs Read Lo-Hi-Lo structure.

33
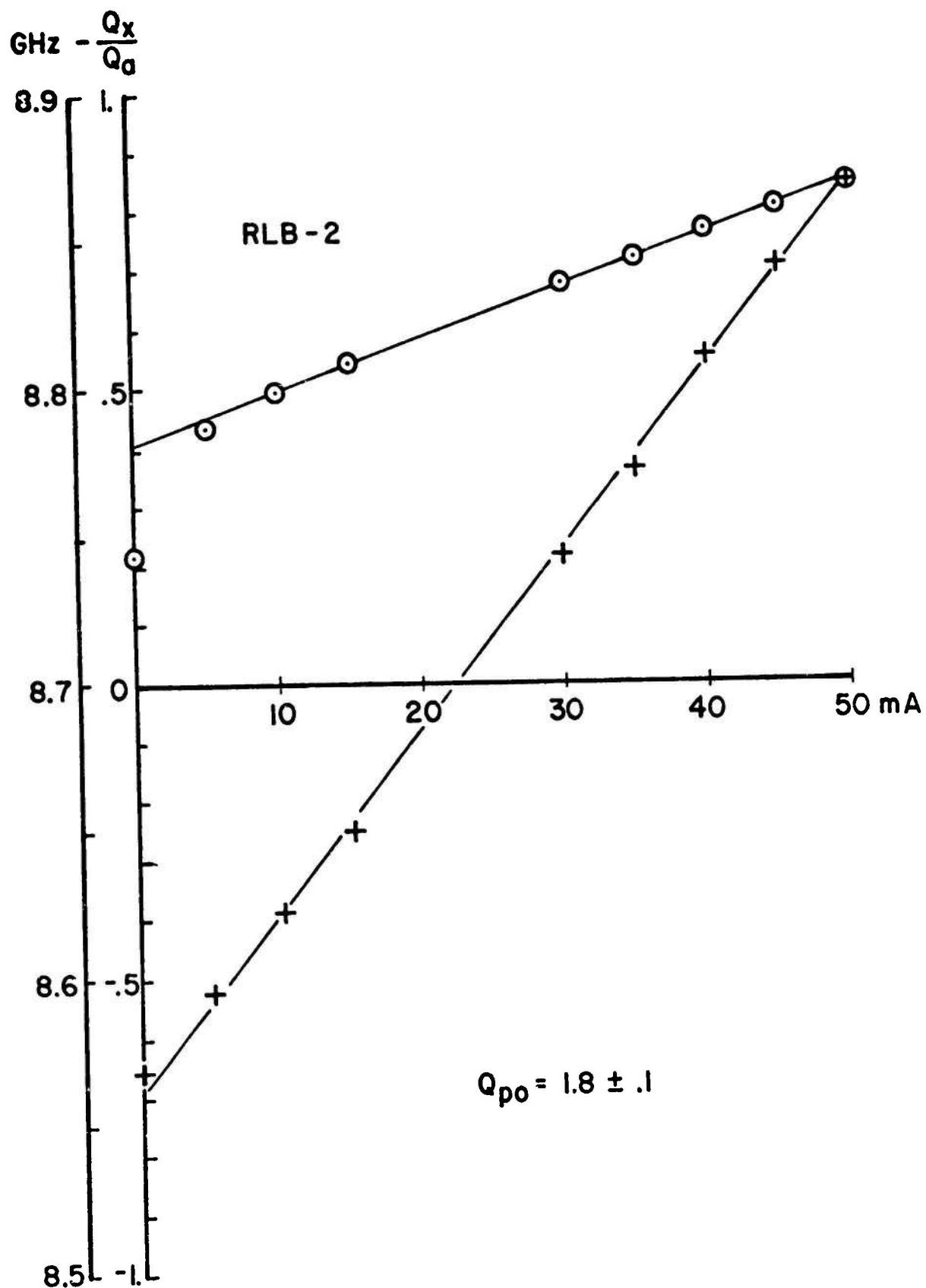
Fig. 3.1-12   Normalized conductance and frequency tuning of the GaAs
Read amplifier of Fig. 3.1-11.

34
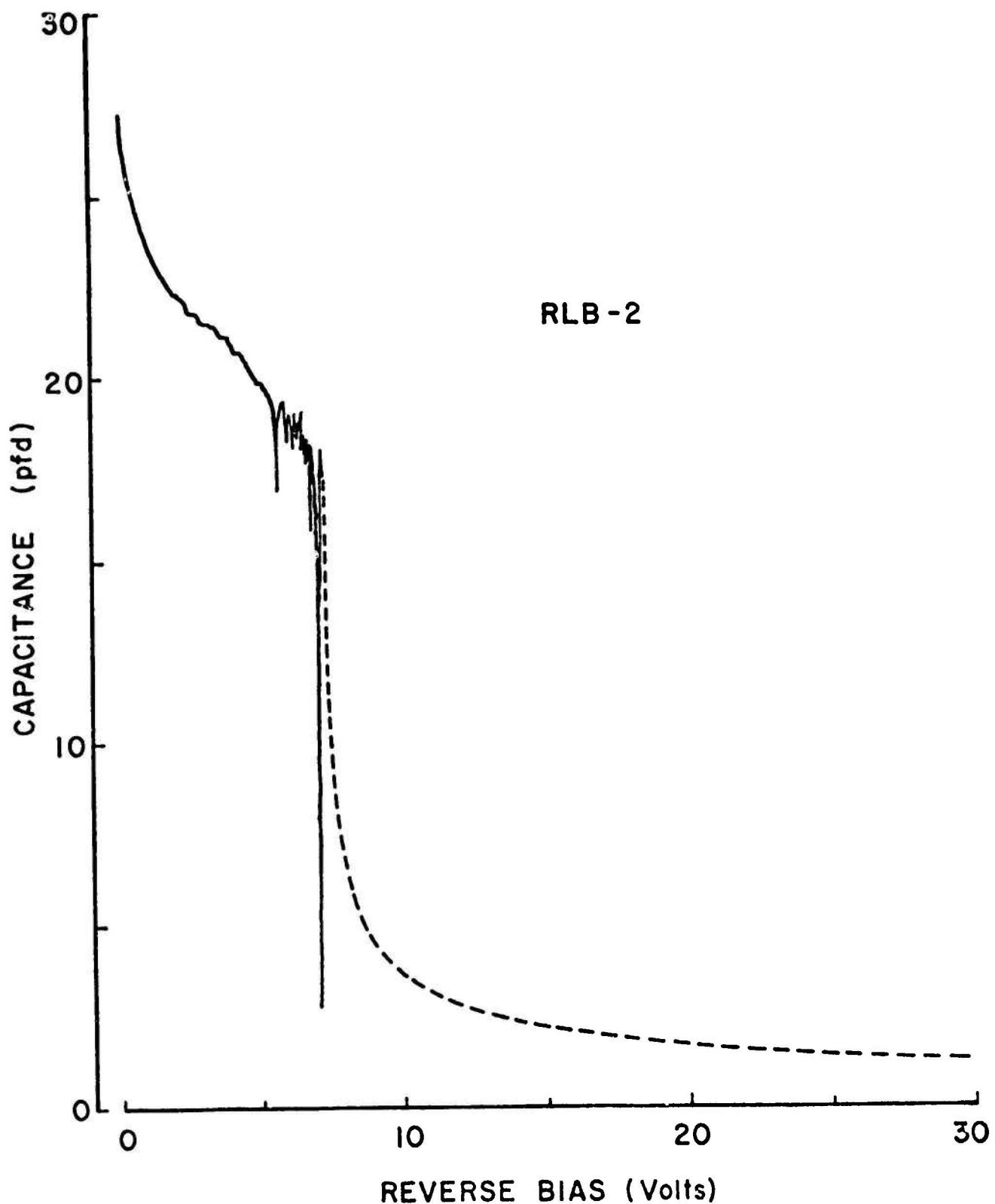
Fig. 3.1-13 Capacitance vs reverse bias of the GaAs Read structure.
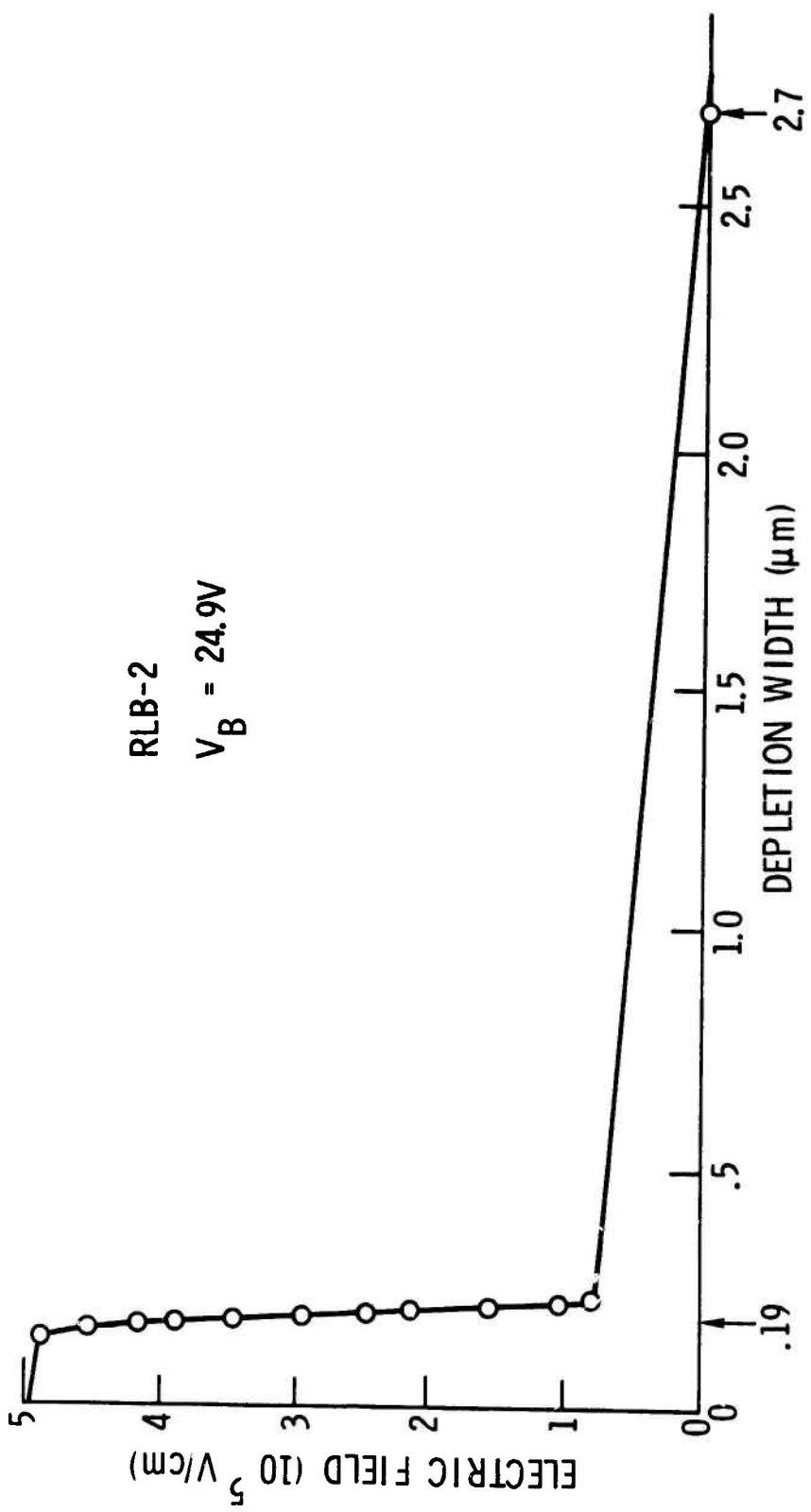
Fig. 3.1-14 Deduced electric field vs distance variation of the GaAs Read diode at breakdown.
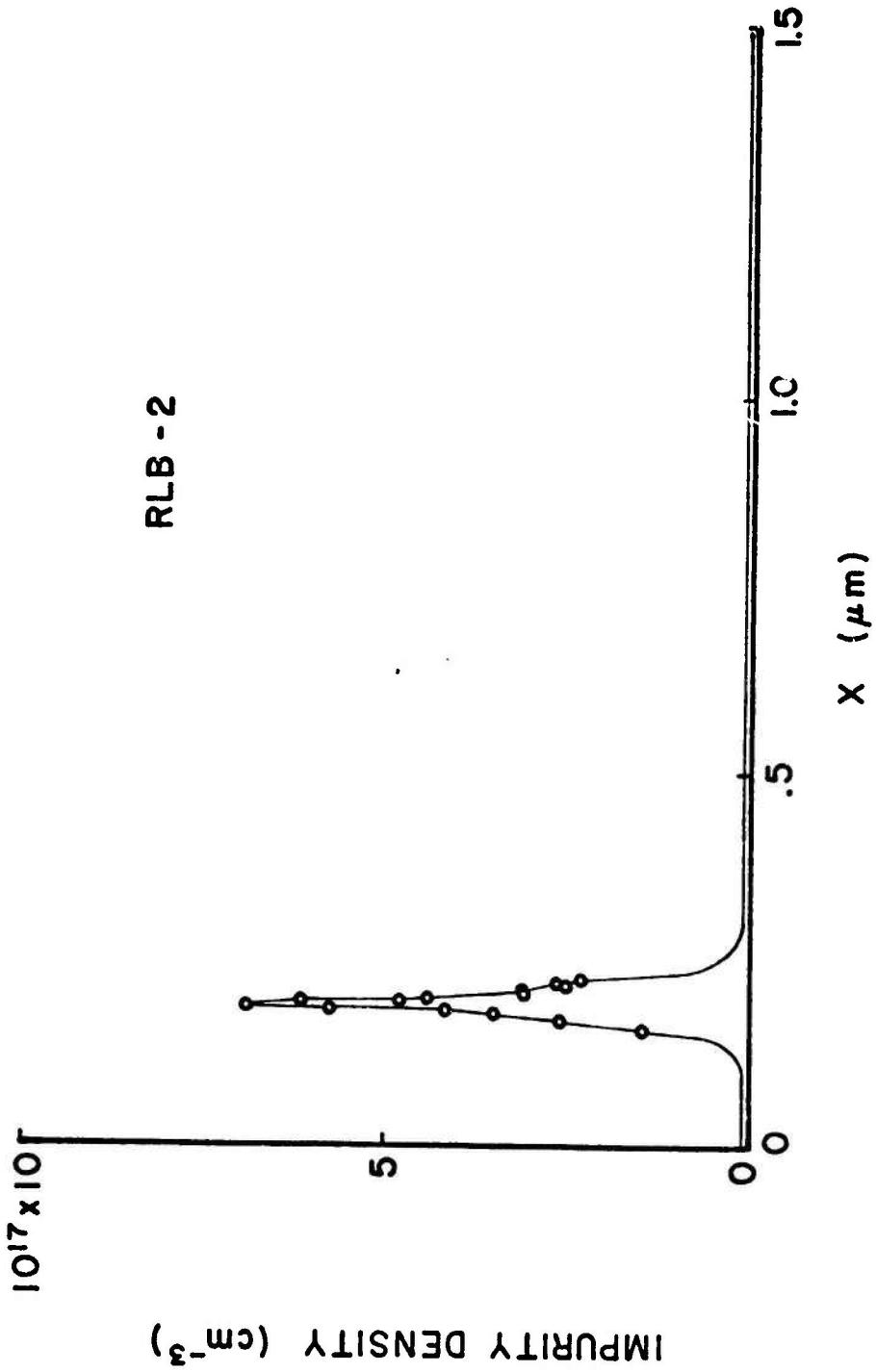
Fig. 3.1-15 Deduced doping vs distance variation of the GaAs Read diode.

data of Fig. 3.1-11, yielding Q_{po} = .6 compared to the measured value of 1.8 $\pm$ .1. In addition, measurements of Q_{po} at lower frequencies show a much stronger variation with frequency than can be accounted for.

There are, of course, a number of simple things that could be different, such as the assumption of uniform doping in the "Lo" drift region, but it is clear that voltage modulation of the space charge width will increase Q_{po} both for the current perturbation and for large ac signal perturbation. Evidence for the latter has been given recently by Kuvås and Schroeder.[7] Other effects not yet taken account of are the electric-field-dependent generation occurring at the defects in the Hi-region and the effect of the inherent inhomogeneity of these defects.

3.1.2.4 <u>Active-Buffer Layer Interface Annealing Study</u>. In the previous report[3] we discussed dimpled punch-through diodes that exhibited enormous increases in saturation current when a high electric field penetrated the interface between the active layer and the buffer layer. This interface problem is a very serious one in GaAs avalanche diodes and has prom`ed the present annealing study to separate the electrical and physical interfaces.

In examining the annealed wafers, one of which was annealed at Rockwell with an A&N cap for $\sim$ 2 hours at 850°C and the other at Cornell for 5 hours at 837°C, a partial success has been observed. One of the diodes on the Rockwell-annealed sample had a breakdown

voltage of 20 volts. Capacitance measurements which were
made on that diode are shown in Fig. 3.1-16 along with the
capacitance profile of a similar diode made on an unannealed
portion of the original wafer. The corresponding doping pro-
file of the good annealed diode is shown in Fig. 3.1-17. At
20 volts reverse bias the current was beginning to grow. Since
the electric field is approaching 2×10^5 V/cm, an attempt was
made to observe secondary multiplication in the diode without
success. Using published ionization rates and a field of 2×10^5
V/cm, we calculate a multiplication of only 1.006 so it is, per-
haps, not surprising that multiplication was not observed. This
one diode, however, showed a considerable improvement in with-
standing high fields at the interface compared to unannealed
ones.

In examining the structure of the diodes, it was found that the
first annealing schedule was marginal. The original wafer had a
buffer layer of $N_d \simeq 10^{17}/cm^3$ approximately 40μm thick doped
with tin on which was grown an active layer doped in the middle
10^{14} range. Originally we had thought the buffer layer doping to
be around $10^{18}/cm^3$. For the higher doping level the annealing
schedule would have given a reasonable separation of the electri-
cal and physical interfaces, but for $10^{17}/cm^3$ doping in the buffer
layer, the annealing was marginal.
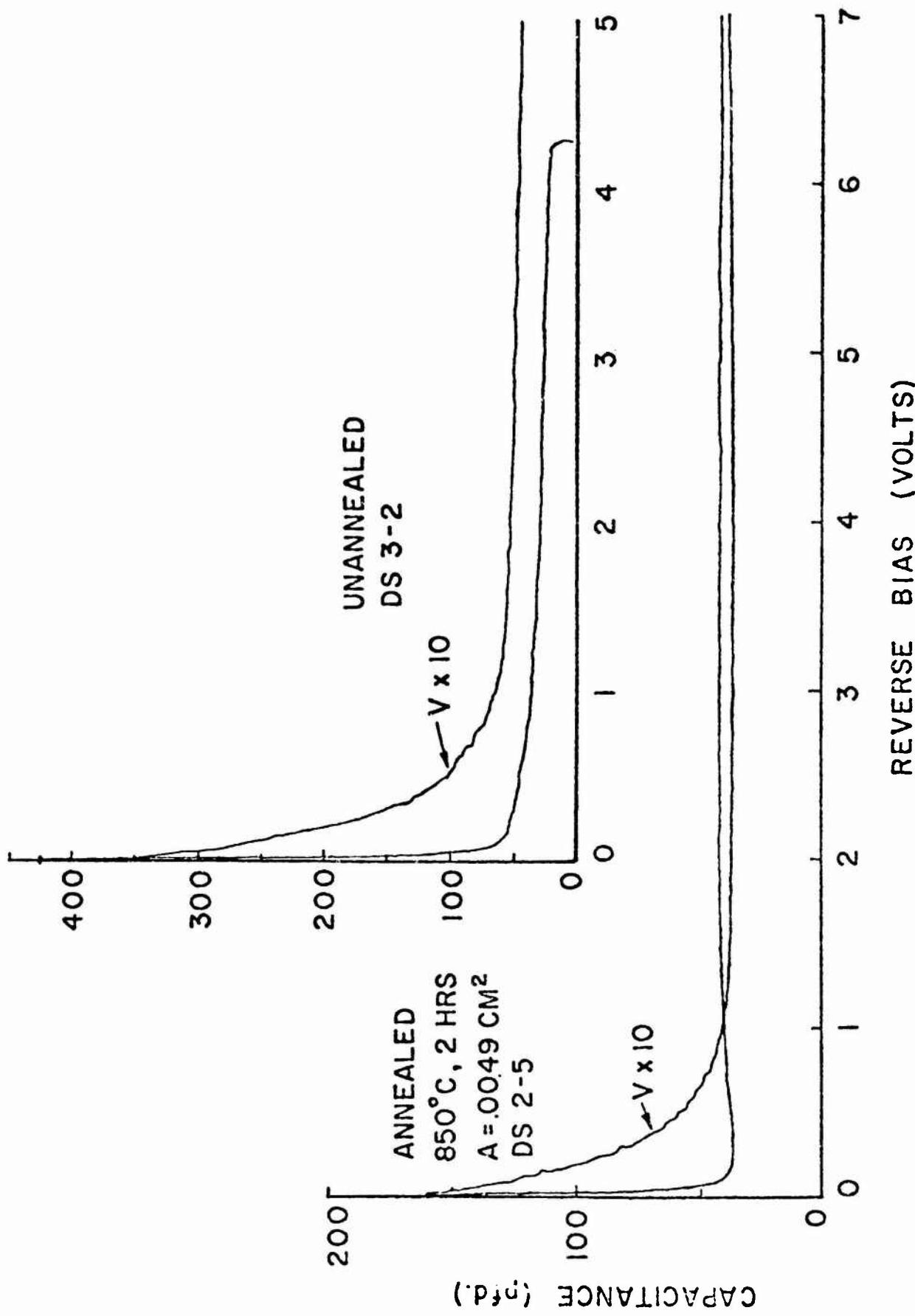
Fig. 3.1-16 Capacitance vs voltage traces of Schottky barrier diodes on portions of an unannealed epitaxial wafer and of diodes on a portion of the wafer annealed at 850°C for 2 hours. The breakdown of the annealed diode is ≳ 20 volts.

40
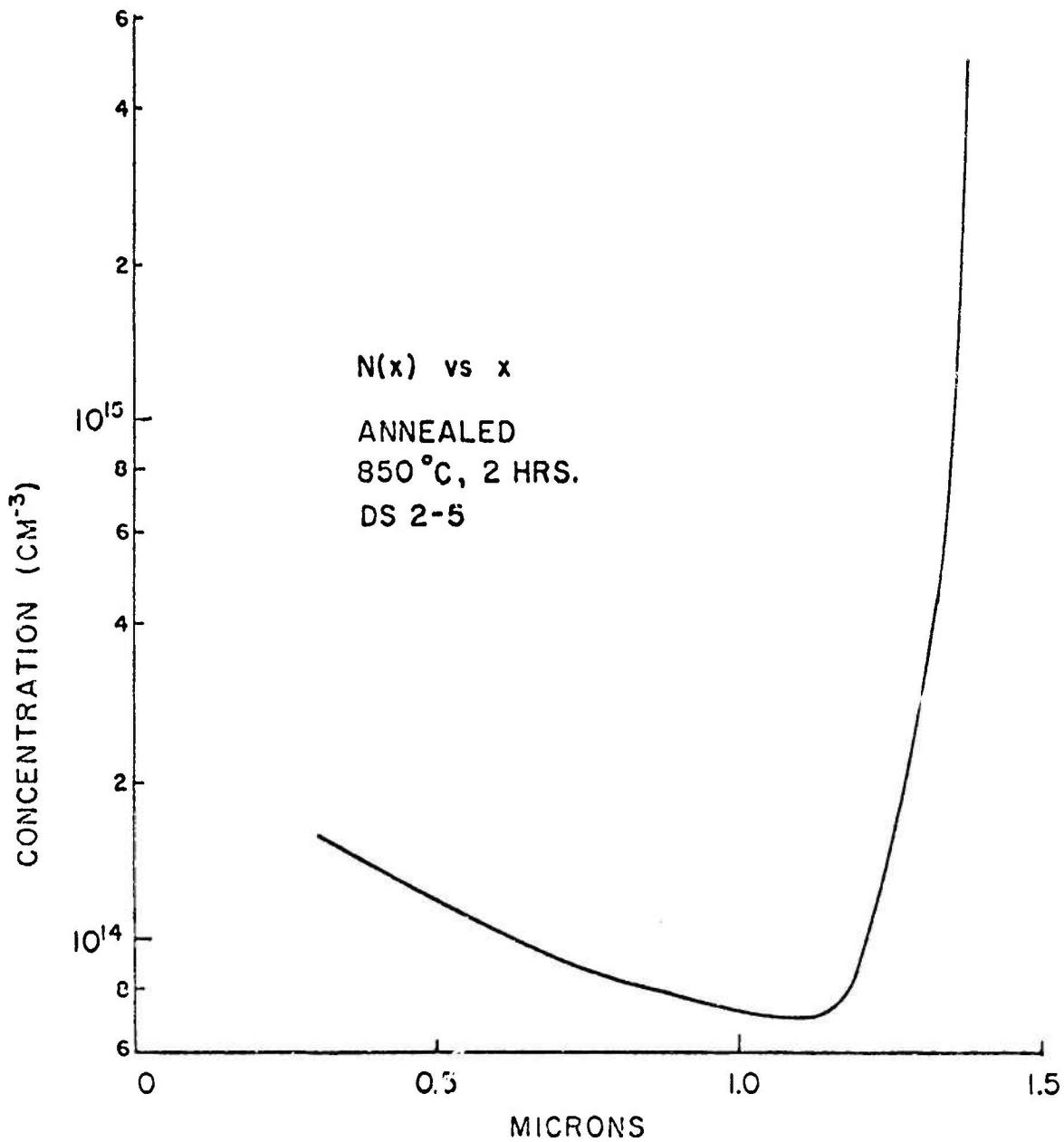
Fig. 3.1-17 Donor density profile of the annealed diode shown in Fig. 3.1-18.

In re-examining the problem, the annealing criterion has been looked at differently. If one wishes to terminate a field of say 2×10^5 V/cm then the edge of the space charge region ($\mathcal{E} = 0$) should still be a half micron away from the physical interface. We start with a step distribution of impurities located at the physical interface ($x = 0$). After annealing for a given time at some temperature the point at which the diffused distribution from the buffer layer is equal to the active layer doping is located (x_2). Then integrating over the diffused distribution to some value of $x = x_3$ at least $.5\mu$m from the interface we find a sufficient number of impurities to terminate a desired field in the active layer. The quantitative expression derived is

$$\mathcal{E}_2 = \frac{qN^+ 2\sqrt{Dt}}{2\varepsilon} \left| \xi_2 \text{ erfc } (\xi_2) - \xi_3 \text{ erfc } (\xi_3) \right.$$

$$\left. + \frac{1}{\sqrt{\pi}} e^{-\xi_3^2} - e^{-\xi_2^2} \right| \quad , \tag{17}$$

where $\mathcal{E}_2$ is the field to be terminated, N^+ is the buffer layer doping, $\xi_2 \equiv x_2/2\sqrt{Dt}$, and $\xi_3 \equiv x_3/2\sqrt{Dt}$.
As a consequence of the lower buffer layer doping of $10^{17}/cm^3$ and Eq. (17), the annealing temperature must be at least 900°C for at least 4 hours.

The encapsulating technique has been improved by covering the
sample with crushed undoped GaAs. It is now possible to anneal
a wafer in the quartz ampoul: at 950° for 8 hours without any
observable change in the polish-etched surface. Several more
samples have been annealed at the higher temperature of 900°
and are presently being evaluated.

Recently, material grown at the Science Center for annealing
studies (slice S11-5) has shown that the interface is exceptionally
free of generation defects. A number of diodes punch through at
about 15 volts (Fig. 3.1-18) and can be stressed out to 40 volts
where the interface field is in excess of 10^5 V/cm. These diodes
show good multiplication (Fig. 3.1-19) and should yield good data
on ionization rates.

3.2 Semi-Insulating Materials

3.2.1 Crystal Growth

The horizontal Bridgman and the gradient freeze techniques of
producing GaAs show advantages such as lower cost of production, uni-
form crystal shapes and generally superior quality of the material pro-
duced. For this reason the horizontal growth methods are slowly emerging
as the primary source of GaAs for both the opto-electronic and microwave
industries.

The major difficulty with the horizontal method is that the
quartz used in the growth process is heated to temperatures above 1247°C.
At these temperatures there is a dissociation of the quartz causing a
contamination of the melt by silicon.

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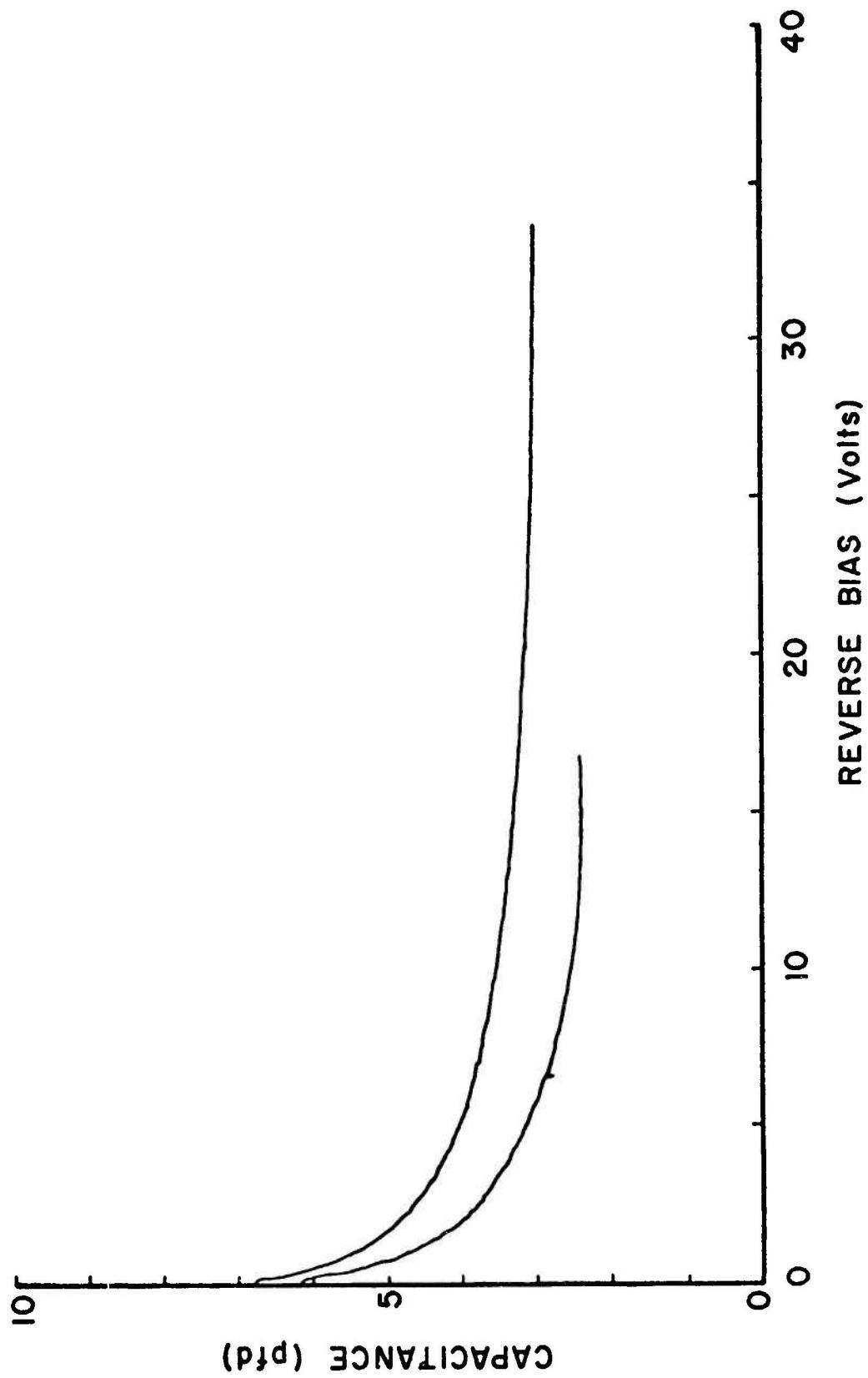
Fig. 3.1-18 Capacitance-voltage recording of two Schottky barrier diodes on Rockwell material.

44
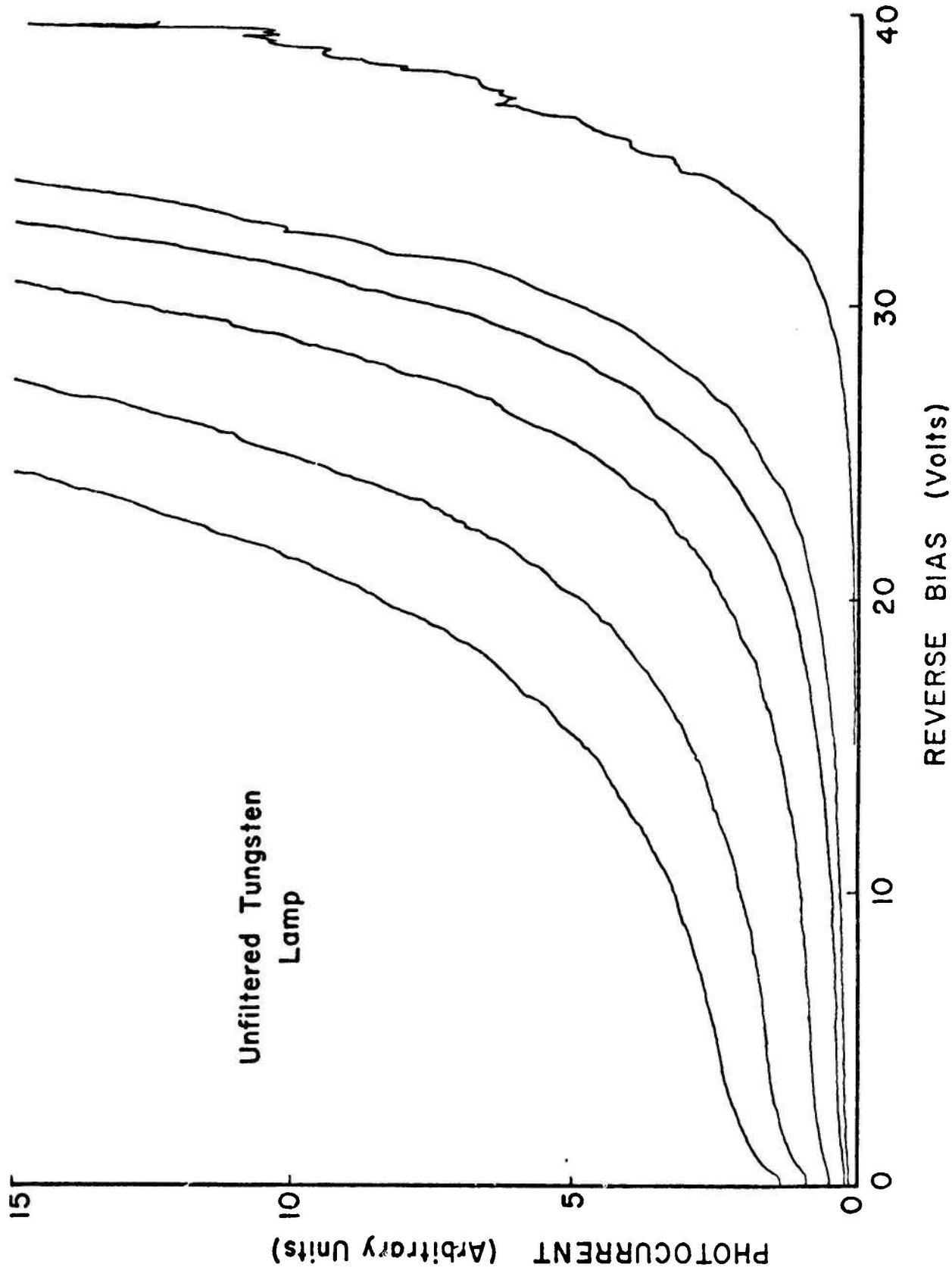
Fig. 3.1-19 Multiplication curves for varying light intensity of the mesa recorded in Fig. 3.1-18.

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Cochran and Foster[8] have described the incorporation of Si into the GaAs by the following reaction:

$$4Ga \text{ (in GaAs)} + SiO_2 \rightarrow 2Ga_2O \text{ (vapor)} + Si \text{ (in GaAs)}$$
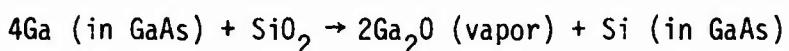
It was reported by Ainslie, Blum and Woods[9] that with the deliberate addition of O_2 to the GaAs melt, the incorporation of Si could be reduced. It was noted by J. M. Woodall[10] that not only was it necessary to add O_2 to the GaAs growth chamber, but it was also necessary to raise the arsenic reservoir temperature above 1140°C. Woodall also found that GaAs with Si contamination up to 1×10^{16} atoms/cm^3 could be compensated if temperatures above 1140°C were maintained during solidification.

It would appear that O_2 serves two roles in producing high resistivity GaAs. One is the reduction of silicon contamination by reducing the dissociation of the quartz boat and ampoule. The second is that of compensation.

Additions of O_2 to the melt after contamination with silicon does not appear to reduce the silicon content of the GaAs. Work at the University of Southern California showed that when GaAs was purposely doped with silicon and later regrown in an O_2 atmosphere there was no measurable decrease in Si content.[11] Local mode studies on this material did not show any measurable decrease in silicon or any impurity pairing. The fact that no absorption bands involving O_2 with Si were observed

does not necessarily rule out compensation at low concentrations. It may be that O_2 does not go into GaAs in sufficient amounts to be observed by this technique.

Preliminary work done at Crystal Specialties shows that high-resistivity GaAs can be produced by using O_2 to prevent the incorporation of silicon. When O_2 was added to the growth chamber prior to reaction of the gallium and arsenic, material with no detectable impurities, other than Aℓ (6.8×10^{15}/cm^3), O_2 (7.7×10^{16}/cm^3) and C (1.8×10^{17}/cm^3) was produced. The probable presence of carbon and oxygen in the mass spectrum background makes the absolute values of the reported concentration uncertain. The mass spectra showed no detectable silicon which is normally found in Bridgman-grown GaAs. After annealing, Hall measurements revealed a resistivity of 8.5×10^6 ohm-cm, a carrier concentration of 5.8×10^8 cm^{-3}, and a mobility of 1270 cm^2/volt-sec. This material was produced by holding the coolest portion of the growth ampoule to 900°C rather than 1140°C as reported by Woodall.[10] With the O_2 pressure lowered, it would be expected that less O_2 would be incorporated into the melt.

The addition of O_2 into the growth ampoule by using Ga_2O rather than gaseous O_2 was attempted. It was felt that this would allow a more accurate measurement of the amount of O_2. A number of crystals were grown using this approach. When Ga_2O was added directly to the growth chamber in place of O_2, the growth of semi-insulating material proved unreliable. Crystals grown using Ga_2O had a free carrier concentration of between 9×10^9 and 3.6×10^{15} cm^{-3} which resulted in a resistivity of 1×10^5 to 0.35 ohm-cm.

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It is probable that when Ga_2O is used instead of direct O_2 there is Si contamination produced during the reaction of the gallium and arsenic. The contamination is caused because it is necessary to keep the arsenic end of the growth chamber below 600°C during reaction to prevent an explosion of the quartz ampoule due to excessive arsenic pressure. By adding O_2 directly to the melt, sub-oxides of As and Ga are formed which are evidently more efficient in reducing Si contamination at lower temperatures.

In Table 3.2-1 the effects of oxygen and Cr + oxygen on the resistivity, carrier concentration and mobility of Bridgman-grown GaAs are compared. It is shown by comparison with ingot No. 1659 (which is typical for undoped crystals) that in all cases of Ga_2O doping the carrier concentration is reduced considerably. However, only in the case of Cr + O_2 additions does the crystal become compensated sufficiently to produce 1×10^7 ohm-cm material.

It is quite evident that the roles played by Cr and O need further clarification.

Table 3.2-1 Compensation of O_2 and $Cr + O_2$ Doped Crystals of GaAs

Ingot No.	Dopant	Resistivity ohm-cm	Carrier Concentration $1/cm^3$	Mobility $cm^2/volt-sec$
1659	None	0.026	7×10^{16}	3420
1921	O_2	1.4×10^5	9×10^9	4900
1922	O_2	1.5	2.2×10^{15}	2830
1939	O_2	0.35	3.6×10^{15}	1742
1945	O_2	5.6	3.1×10^{15}	1972
1970	O_2	0.63	1.6×10^{15}	6140
1971	$Cr + O_2$	1.8×10^7	1×10^{15}	3700
1975	$Cr + O_2$	3×10^7	---	----

Note: Oxygen was introduced in the form of Ga_2O

3.2.2 Material Evaluation

Although the problem of characterization of semi-insulating GaAs was already discussed in earlier reports, it is worthwhile to briefly review some of the difficulties associated with this problem. Lack of sufficient characterization is best expressed by the fact that the only electrical parameter that can be specified today for semi-insulating GaAs is the resistivity. This parameter is certainly not enough. For some device applications, it is necessary to know the densities of electrically-active impurities in order to be able to determine the

electrical behavior of the junction between the epitaxial layer and the device. Better characterization of the substrate material is also being required by the ion implantation technique which for many applications depends on implants in semi-insulating material.

The measurement of densities of electrically-active impurities is a difficult problem in semi-insulating GaAs. Hall resistivity measurements, excellent tools for semiconductors with shallow impurities, are of little help because there is no direct relationship between density of free carriers and density of deep impurities in a compensated semiconductor. There is some considerable amount of information on deep impurity levels from photoconductivity,[12] optical absorption,[13] and related techniques. But these techniques do not supply the needed quantitative information.

It was apparent from the beginning of this contract that injection techniques[14] could be used to measure densities of electrically-active impurities because such techniques yield directly the total amounts of fixed charges that can be trapped in the material. However, injection measurements can be used reliably only when it is sure that one type of carrier at a time is injected into the material. Uncertainty on whether there was double injection affected our early measurements on n-i-m structures, and also made questionable some injection measurements published in the literature on semi-insulating GaAs.[15]

The risk of double injection was excluded by no longer using metal contacts and constructing, instead, n-i-n and p-i-p structures. In addition, it

was decided not to relay on diffused contacts,[15] but rather to grow
two epitaxial layers, one on each side of the substrate. The substrates
were thinned to 20 to 80µm by etching, after the first layer was grown.
A schematic of a p-i-p structure is shown in Fig. 3.2-1. The n-i-n
structures are made in similar fashion. Dopants for the epitaxial layers
are Sn for the n-i-n samples and Ge or Si for the p-i-p structures. The
two-side epitaxial growth makes the construction of the samples diffi-
cult, but it was necessary in order to reach conclusive results.

A sample design that excludes double injection is not enough to
guarantee that the injection model is valid. It is conceivable that one
of the contacts may be a blocking contact. In this event, the I-V
characteristic is determined by this reverse-biased junction rather than
by transport of carriers injected by the opposite contact through the
sample. An example of depletion behavior would be an n^+-π-n^+ structure,
while injection behavior would be expected from an n^+-ν-n^+ structure.

An ideal way to distinguish between injection and depletion
behavior of a sample is to measure the voltage profile across the
sample. Although this is usually an impossible task with current
means, we found a way to make such a measurement of the potential pro-
files across the p-i-p and n-i-n samples by a novel application of
Auger electron spectroscopy (AES) developed at the Science Center.
This is the first time the AES technique has been applied to semicon-
ductor junctions for voltage profiling. In AES, an exciting beam of
electrons of several keV energy (the primary beam) is directed at the
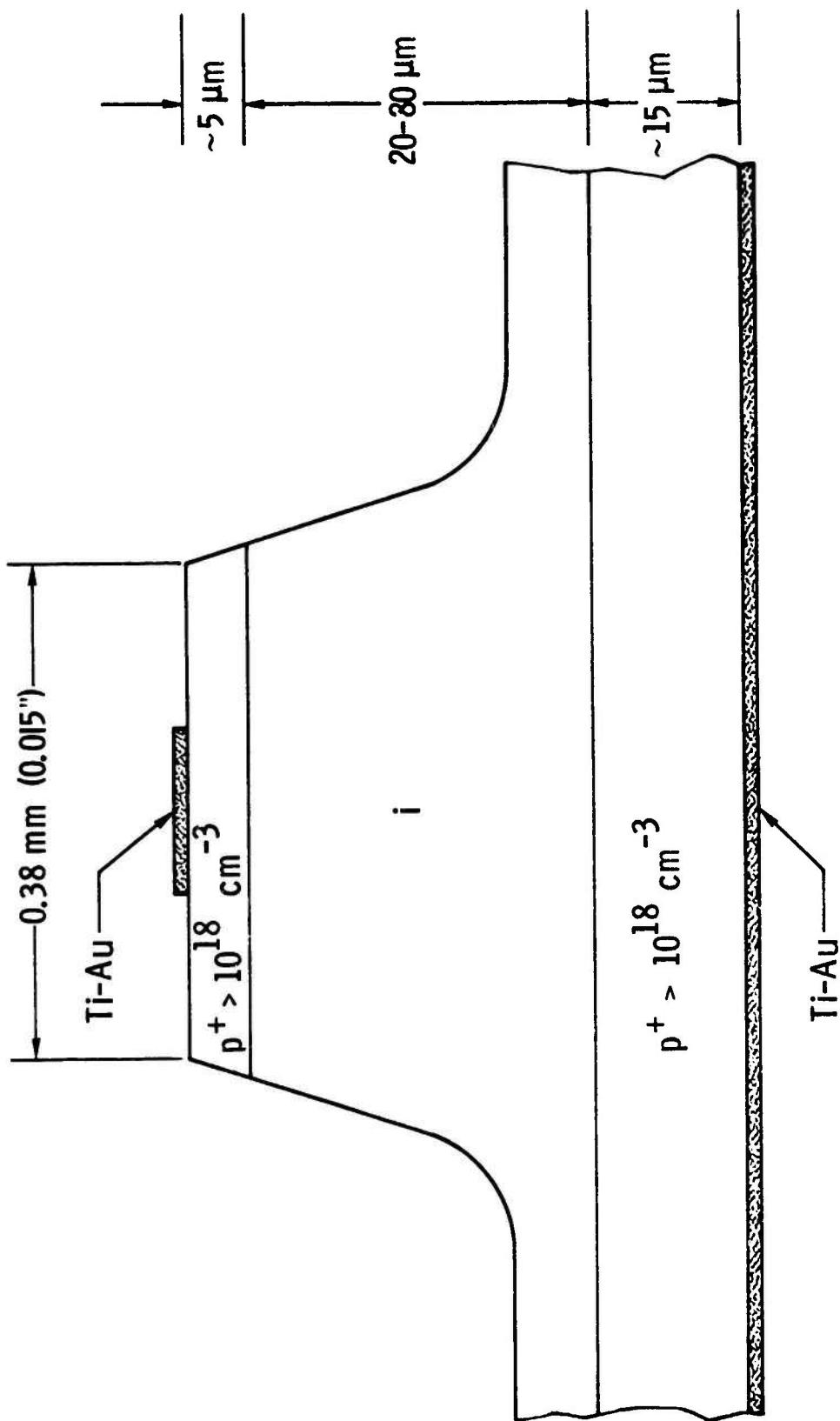
Fig. 3.2-1 Schematic of a p-i-p structure.

~5 μm

20-80 μm

~15 μm

0.38 mm (0.015")

Ti-Au

$p^+ > 10^{18}$ cm^{-3}

i

$p^+ > 10^{18}$ cm^{-3}

Ti-Au

surface of a solid and the resulting secondary electron spectrum is energy-analyzed with an electron spectrometer. Over the energy range of 0-1500 eV the secondary electron spectrum exhibits discrete peaks (hence, Auger electron spectrum) whose positions are characteristic of the particular elements present in the surface region excited. It has been demonstrated, however, that a given Auger electron peak will shift linearly in energy in direct correspondence to an electrical potential applied to a specimen.[15] If the relative shift of a peak at different points across a dc-biased specimen is measured using high spatial resolution AES, the potential profile across the specimen can be obtained.

Our experiments employ an ultra-high-vacuum (10^{-10} torr range chamber pressure) scanning electron microscope (SEM) recently constructed in this laboratory for high spatial resolution ($< 1\mu m$) AES work. Other instrumentation details are similar to the AES-SEM systems previously described.[16,17] Operating parameters for the AES-SEM system during the experiment were 20 kV beam voltage, 20 nA beam current, and 9×10^{-10} torr chamber pressure. Spatial resolution in the potential measurement and the micrograph is $\sim 0.75\mu m$. The accuracy of the potential measurement is ~ 1 volt.

The procedure is to first use the system as a SEM to obtain a secondary electron micrograph of the specimen over a region of inter-est. Next, the finely-focused ($< 1\mu m$) primary beam of the SEM is com-puter-controlled to digitally step in a sequence of discrete points along a chosen line on the specimen. At each point, the derivative[18]

of the Auger electron peak of C (or, for some sequences, O) is recorded.
(Any specimen examined by AES, even in an ultra-high-vacuum system such
as ours, will normally have C and O peaks unless specially cleaned under
vacuum.) The shift in energy of the Auger electron peak when voltage is
applied to the specimen is measured for every point. The shifts are then
calibrated against the shifts caused by known potentials applied to a
metal electrode. Then the potential at each point on the line scan can
be associated with the specimen geometry recorded on the secondary
electron micrograph. The technique was tested on a well-characterized
GaAs p-n junction, finding excellent agreement with the predicted profiles
for different bias voltages.[19]

The secondary electron micrograph of a p-i-p structure made with
Laser Diode material is shown in Fig. 3.2-2a. The sample is mounted
sidewise. The points where the potential was measured are indicated.
Absolute values of the potential at these points for a ±15V bias voltage
are shown in Fig. 3.2-2b. The bias is applied to the left side, the
right side is grounded. The behavior of the left-side p-i junction with
respect to applied polarity is striking. With negative applied voltage,
the potential (dots) falls rapidly to zero when moving away from the left
p-i junction. This drop indicates an electric field concentrated near
the junction and zero elsewhere. For positive applied voltage, the
potential (circles) is constant when moving away from the left junction,
and, therefore, the electric field is always zero. Similar potential
profile behavior was qualitatively seen at the right p-i junction.

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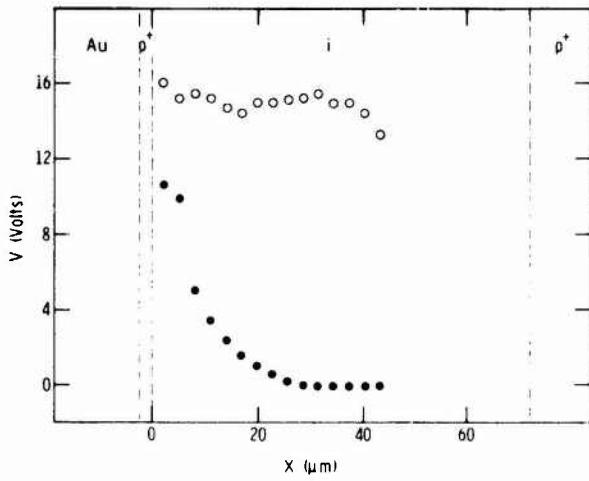
3.2-2 p-i-p structure made with Laser Diode #2639 material.
(a) SEM secondary electron micrograph (the p^+ regions
were identified by cathodoluminescence); (b) absolute
values of the potential. Dots: left side biased
negative; circles: left side biased positive.

The potential profiles of Fig. 3.2-2b suggest that the p-i junctions are acting like forward- and reverse-bias abrupt p-n junctions. This notion was confirmed when the square root of the potential values under negative bias plotted against distance from the left junction (Fig. 3.2-3) showed a linear dependence. The line in Fig. 3.2-3 is a least square fit. From the slope, a density of ionized donors states in the depletion region of $N_D = 2.0 \times 10^{13}$ cm^{-3} is obtained through Poisson's equation.

This is the first observation of a depleted junction in Cr-doped semi-insulating GaAs. Such a depletion effect indicates that the semi-insulating material is behaving as n-type. This n-type behavior is not accidental. Voltage profiles measured by AES on another p-i-p samples, and this one made with Crystal Specialties Cr-doped semi-insulating GaAs have a similar depletion behavior. This can be seen in Fig. 3.2-4 where the square root of the voltage is plotted for different bias voltages and different polarities.

Features in the p-i-p structure I-V characteristic (Fig. 3.2-5) also reflect the existence of a junction depletion region. The sublinear slope in the log-log plot indicates a saturation effect typical of that found in a reverse-biased p-n junction. The punch-through voltage is in agreement with that predicted from the voltage profiles. On the same Fig. 3.2-5, the I-V characteristic of an n-i-n structure made with the same Crystal Specialties material is also shown. Knowing that the
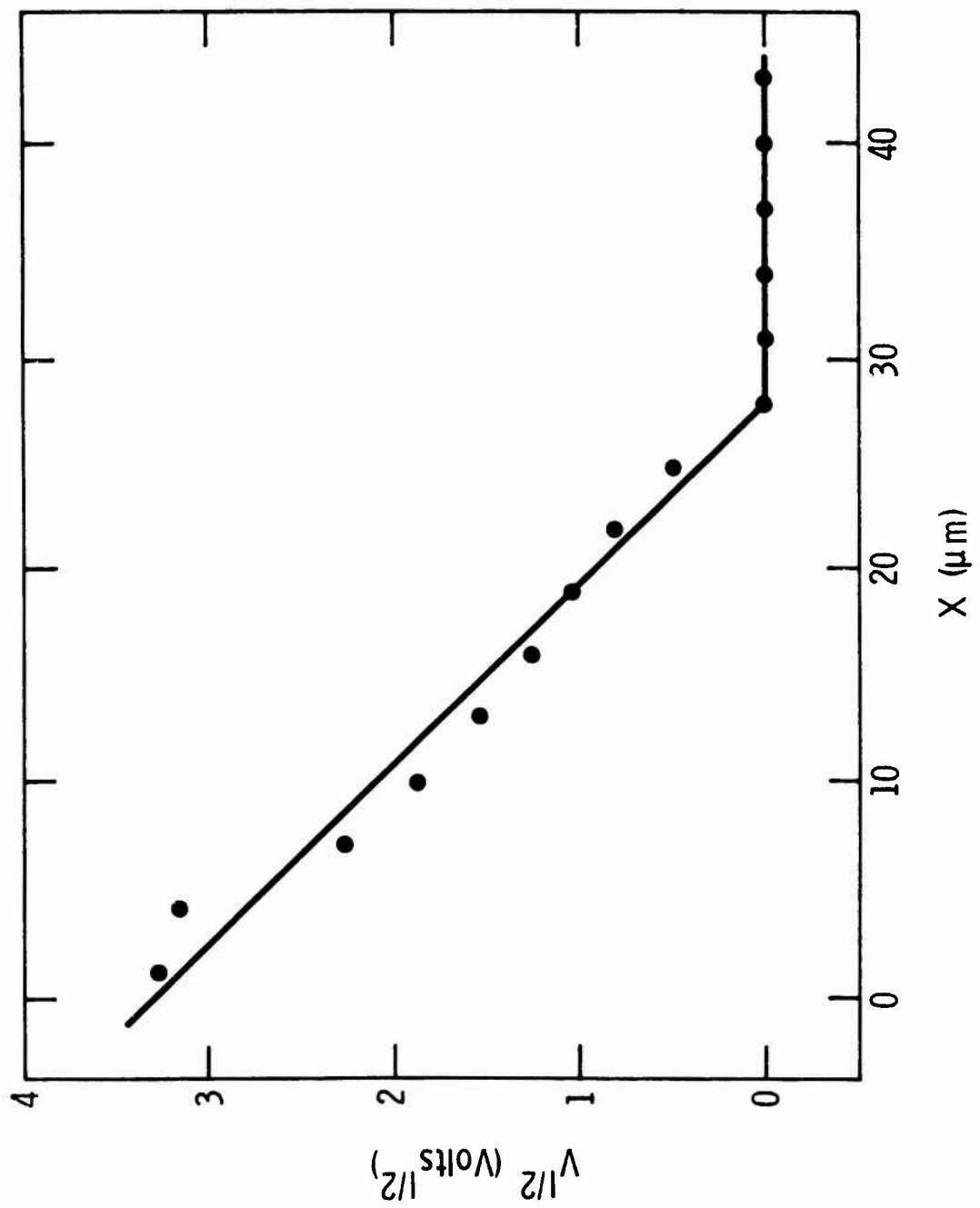
Fig. 3.2-3 Square root of the potential across the p-i-p structure with left side biased negative. Dots: experimental points; line: least square fit.
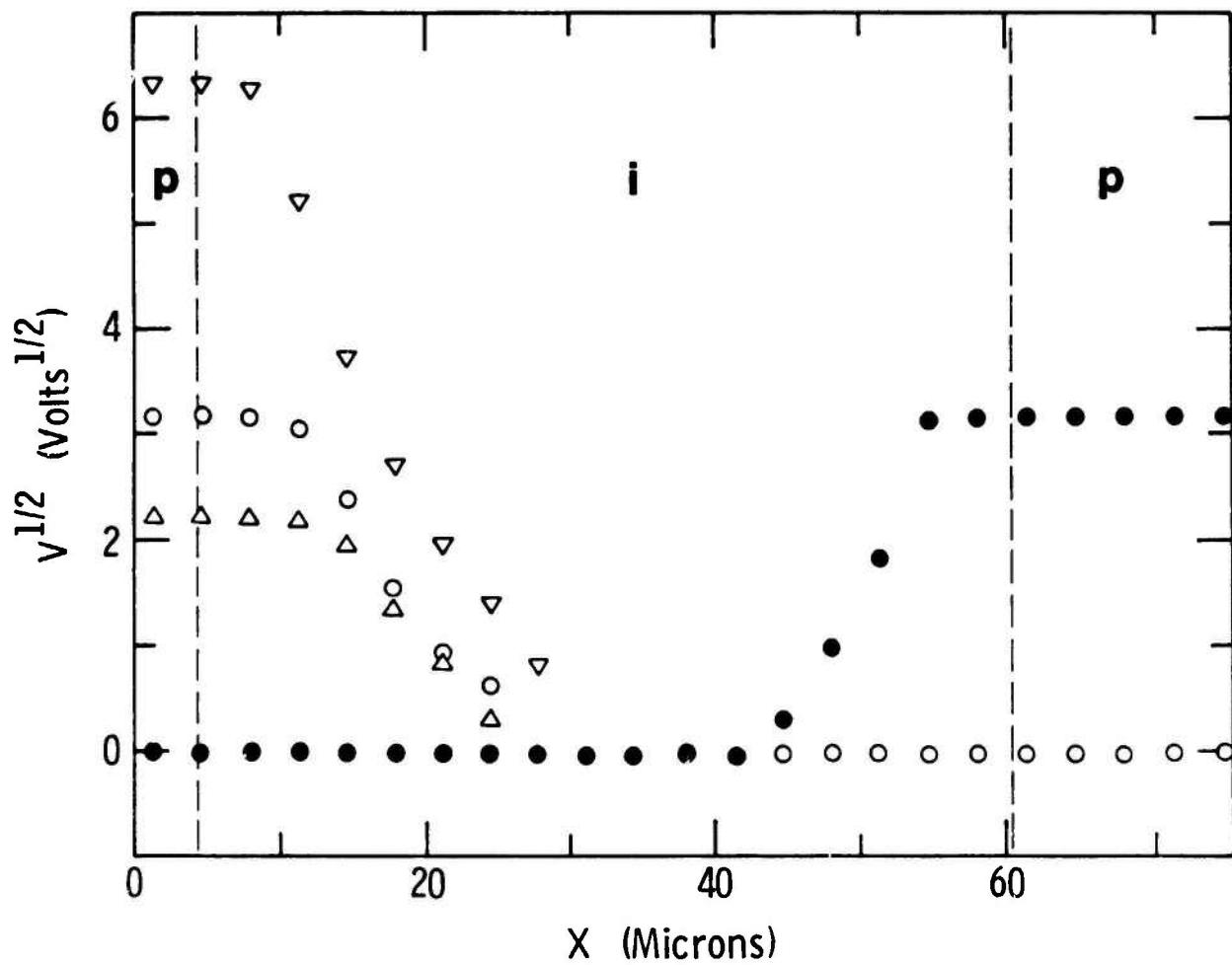
Fig. 3.2-4 Square root of the potential across a p-i-p structure
made with Crystal Specialties #1718 material. Bias
voltages: ∇-40V; O-10V; ∆-5V applied to the left
contact; ●-10V applied to the right contact.
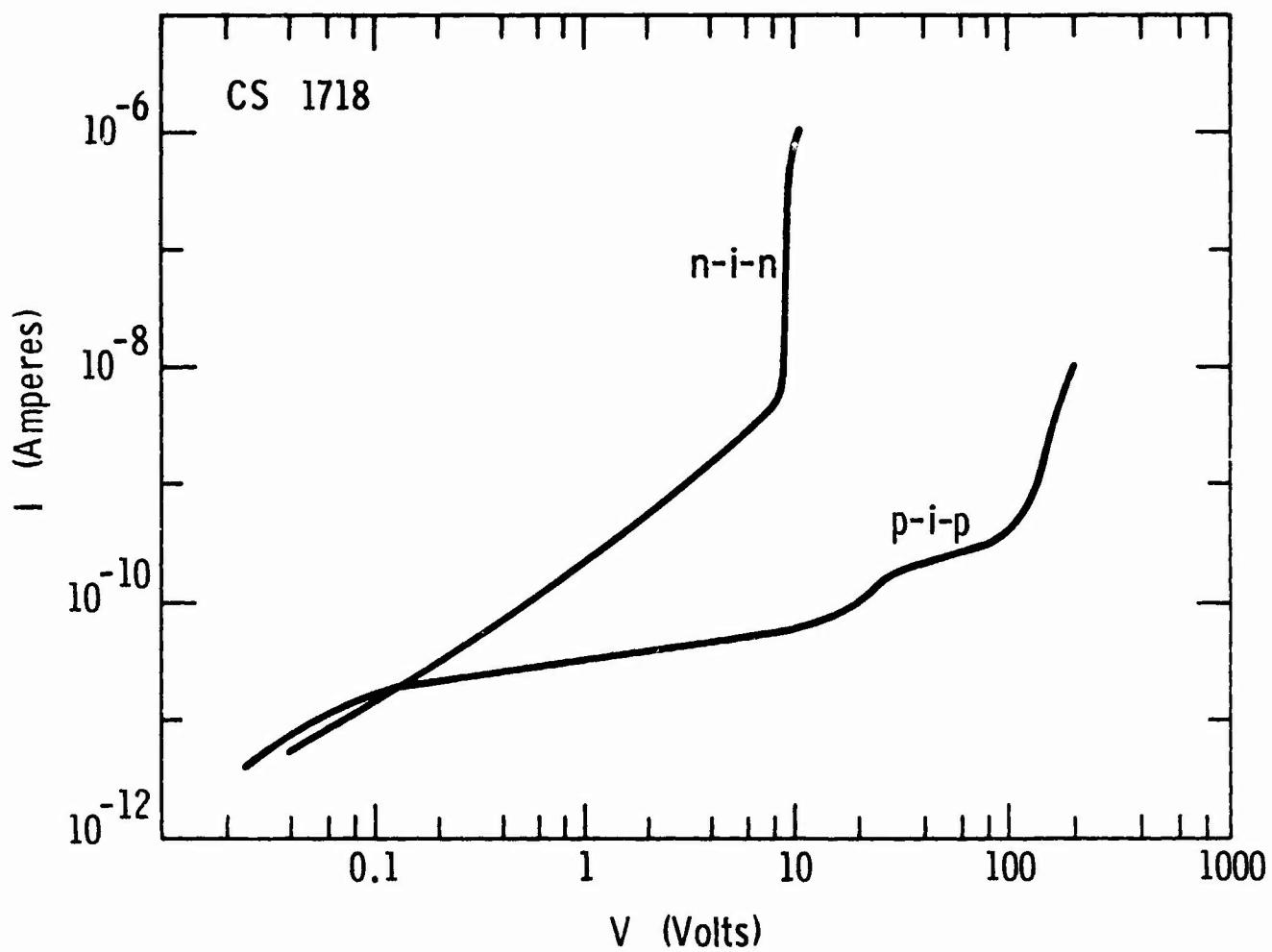
Fig. 3.2-5   I-V characteristics of a p-i-p and an n-i-n structure
(Crystal Specialties #1718 material).

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material behaves as n-type, no depletion is expected. In fact, the
curve is quite ohmic at low voltage. It exhibits a trap-filled-limit
voltage V_{TFL} = 10V.

The different behavior of the n-i-n structures also appears in
the voltage profile. In fact, AES-SEM system measurements on an n-i-n
structure gave a potential profile (Fig. 3.2-6) distinctly different from
the p-i-p results. The n-i-n profile is identically shaped for both
positive and negative polarity bias. This behavior with polarity shows
that no depletion region is formed at either n-i junction. A definite
cause for all potential drop not starting at the n-i boundary line
determined by cathodoluminescence (dashed lines in Fig. 3.2-6) is
unclear. There is a possibility that light Sn diffusion into the SI
GaAs during growth of the heavily Sn-doped layer lowered the resistivity
of the SI GaAs near the n-i boundary. Indeed, a capacitance measurement
at 1 MHz yielded a dielectric thickness of 46µm, more in agreement with
the distance over which the potential profile shows a drop. A similar
although less pronounced effect is seen in the voltage profiles of
Fig. 3.2-4 for a p-i-p structure. This problem requires further systematic
study.

Quantitative results are shown in Table 3.2-2 for the Laser Diode
and Crystal Specialties materials tested. N_D, the density of donor
states, including shallow and deep donors, is equal to the density of
fixed positive charges uncovered in the depletion regions of the p-i-p
structures. It is calculated from the potential profiles. N_A, the
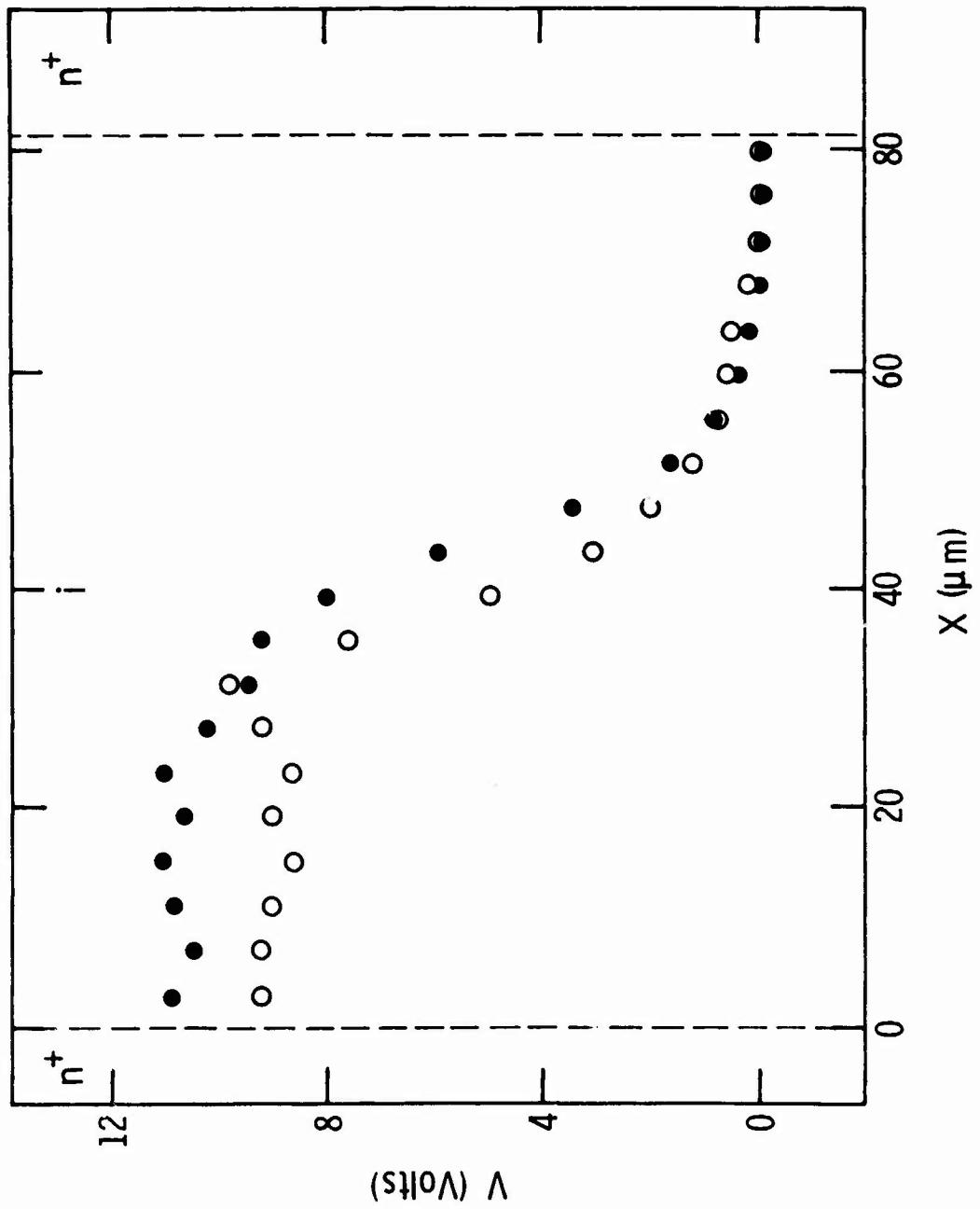
Fig. 3.2-6   Absolute value of the potential across a n-i-n structure made with Laser Diode #2639 material. Dots: left side biased negative; circles: left side biased positive.

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density of acceptor states is equal to the density of electron traps.
It is obtained from the trap-filled limits of the I-V characteristics of
the n-i-n structures.

The densities of acceptor states N_A shown in Table 3.2-2 are low
as our early measurementson n-i-m structures predicted. N_A is also lower
than the density of donor states N_D for both sample materials. This has
repercussions on the model for Cr-doped semi-insulating GaAs shown in
Fig. 3.2-7a, which reflects a quite generalized consensus cn how the
electrical compensation of the material occurs. In this model, Cr acts
as a deep acceptor with a concentration N_{DA} larger than that of the back-
ground shallcw donors N_D, in order to keep the Fermi-level near the
center of the gap. Our observation of more donors than acceptors in
materials with high resistivity ($\rho > 6 \times 10^7$ ohm-cm) invalidates this
model.

Table 3.2-2   Densities of Electrically-Active Impurities
in Semi-Insulating GaAs

|	Laser Diode #2639	Crystal Specialties #1718
N_D From Voltage Profile of p-i-p	2.0×10^{13} cm^{-3}	5.5×10^{13} cm^{-3}
N_A From V_{TFL} of n-i-n	9.5×10^{12} cm^{-3}	2.2×10^{13} cm^{-3}
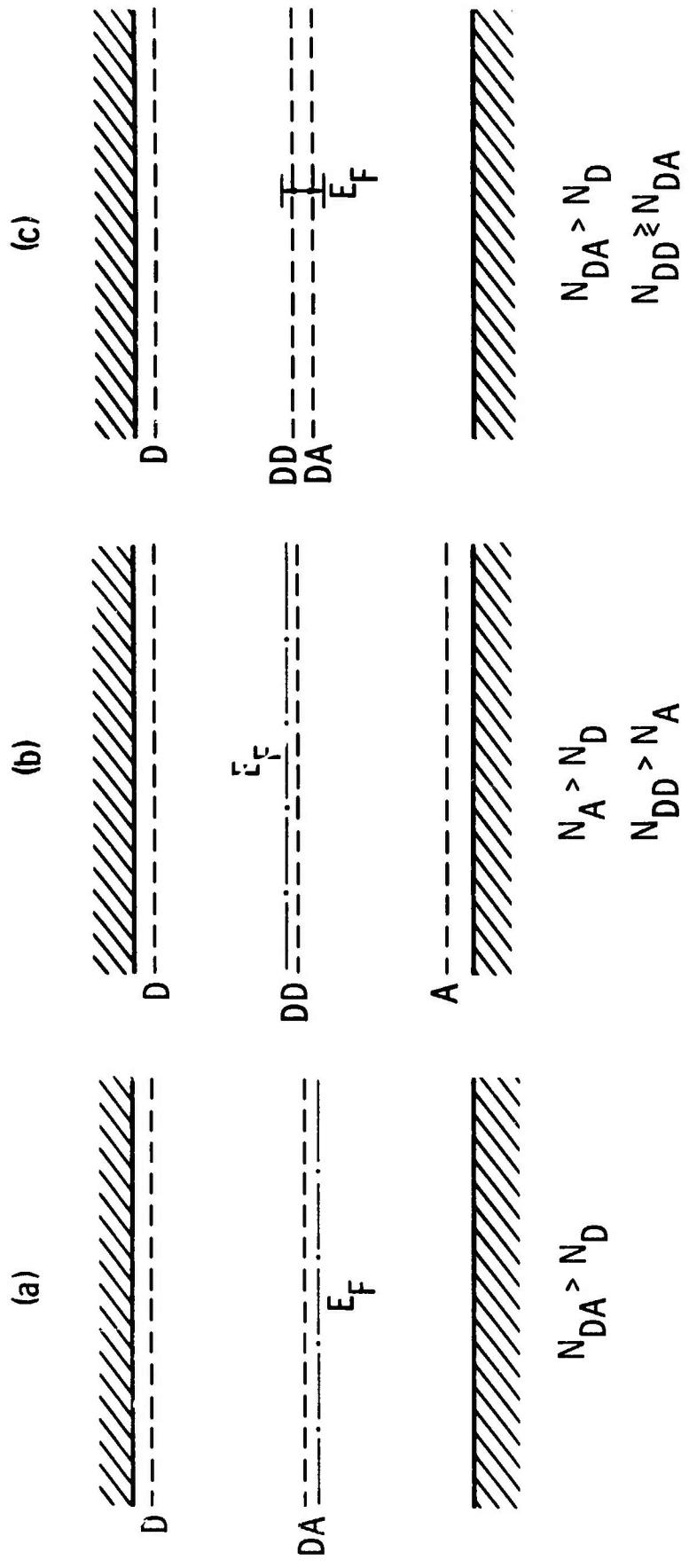
Fig. 3.2-7 Models for the electrical compensation in semi-insulating GaAs.

In the search for a more suitable scheme of electrical compensation, Fig. 3.2-7b shows Blanc and Weisberg's model for O-doped, high-resistivity GaAs.[20],[21] This model requires a shallow acceptor with a concentration N_A higher than that of the shallow background donors N_D. Finally O, acting as a deep donor with a concentration N_{DD} still higher than the acceptor, brings the Fermi level near the middle of the gap. This type of model leads to an n-type behavior.

As was discussed in Sec. 3.2-1, Cr-doped GaAs always contains O in amounts comparable with those of Cr. Therefore, a viable alternative is the model shown in Fig. 3.2-7c, which is like that of Fig. 3.2-7b for the O-doped material, except that the shallow acceptor is replaced by the deep acceptor Cr. The Fermi level is pinned at the middle of the gap by the deep acceptor and the deep donor regardless of which one has a higher concentration. This model corresponds to a material quite stable resistivity-wise against fluctuations of the concentrations of dopants in agreement with the observation that the resistivity is quite stable across a good boule of semi-insulating material. This model was proposed as one among several alternatives by Haisty and Cronin[22] when they introduced Cr doping. A crucial test for the models will be to see how variations of growth conditions will affect the densities of electrically-active impurities.

Still the fact remains that the observed densities of electrically-active impurities are three orders of magnitude below the densities of impurities (O, Si, Cr) measured by mass spectroscopy. It is possible

that a fundamental part of the compensation of impurities takes place
by formation of electrically-inactive complexes.[22,23]

The effect of the results presented here on device design is to
relieve our concern with depletion regions between n-type epi-layers
and substrates, because the substrates examined so far behaved as n-type.
Further work is necessary to verify such behavior more extensively. On
the other hand, the observed penetration of the electrically-active
n-layer into the substrate suggests that interface states must be con-
sidered as a potential source of noise.

In summary, a technique has been developed to measure densities
of electrically-active impurities in semi-insulating GaAs by a combina-
tion of traditional injection techniques and a novel application of
Auger spectroscopy. This technique allowed us to distinguish depletion
from injection behavior of the samples and so to determine that Cr-doped
GaAs behaves as n-type, forming depleted junctions with p-type material.
The measured donor and acceptor densities do not support the widely-
accepted model in which electrical compensation is due to Cr only, but,
rather, it suggests a model with both a deep donor and a deep acceptor.

3.3 Ion Implantation--Results

During the past six months, considerable data have been obtained on the
electron concentration and mobility profiles produced by tellurium ion

implantation doping of GaAs. These experiments have examined the effects of varying implantation dose, anneal temperature, implant temperature, and substrate material. The effects of implanting gallium in amounts equal to or greater than the implanted tellurium, and the profiles obtained with the tellurium beam aligned along (110) planes or aligned in random directions have also been studied. In addition, preliminary results for selenium implantation doping of GaAs have been obtained. In all these experiments, reactively-sputtered Si_3N_4, with properties similar to those described in the previous scientific report,[3] was used as an annealing cap. The stripping technique employing anodization of the GaAs, which was also described in the previous report,[3] was used in carrying out the profile measurements.

Electron concentration profiles for samples implanted with 10^{13} 400 keV Te ions/cm^2 at a temperature of 350°C are shown in Fig. 3.3-1. Data for implantation doses of 10^{14} Te ions/cm^2 are presented in Fig. 3.3-2. In both figures, the tellurium distribution expected for random penetration of the incident tellurium ions, as calculated from LSS[24] range parameters, is shown by the dashed lines. For both doses the maximum electron concentrations obtained increased with increasing annealing temperature. The maximum electron concentrations obtained for an 850°, 120-minute anneal or a 900°, 10-minute anneal are the same for both doses. Except for the 750° anneal data shown in Fig. 3.3-1, the profiles show electron distributions which extend significantly beyond the LSS range curve. The very deep penetration indicated for one sample in each figure may not be typical of tellurium
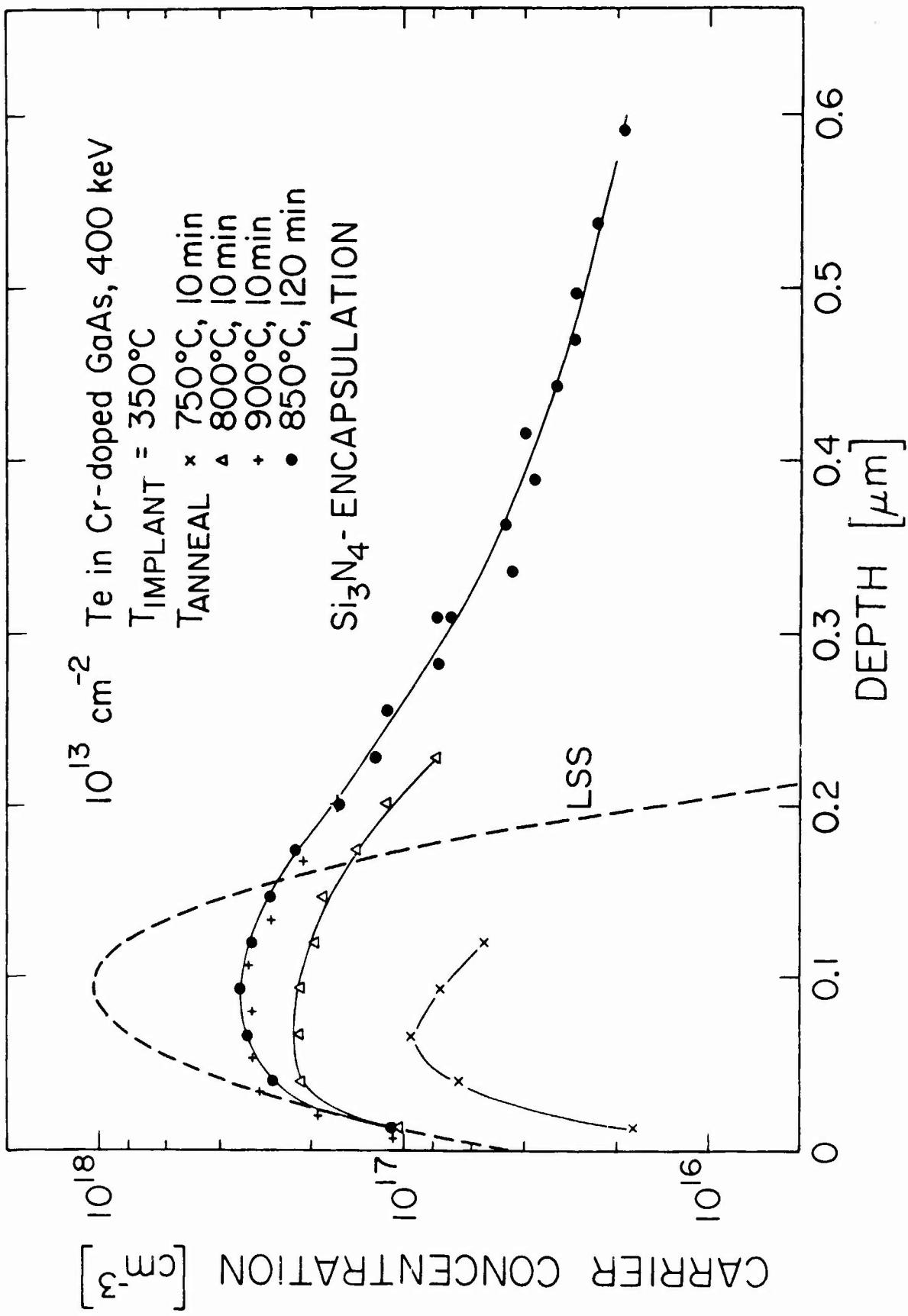
Fig. 3.3-1 Electron concentration profiles for semi-insulating GaAs, samples implanted
with 400 keV tellurium ions at 350° to a dose of $10^{13}/cm^2$, and annealed
at the indicated temperatures.
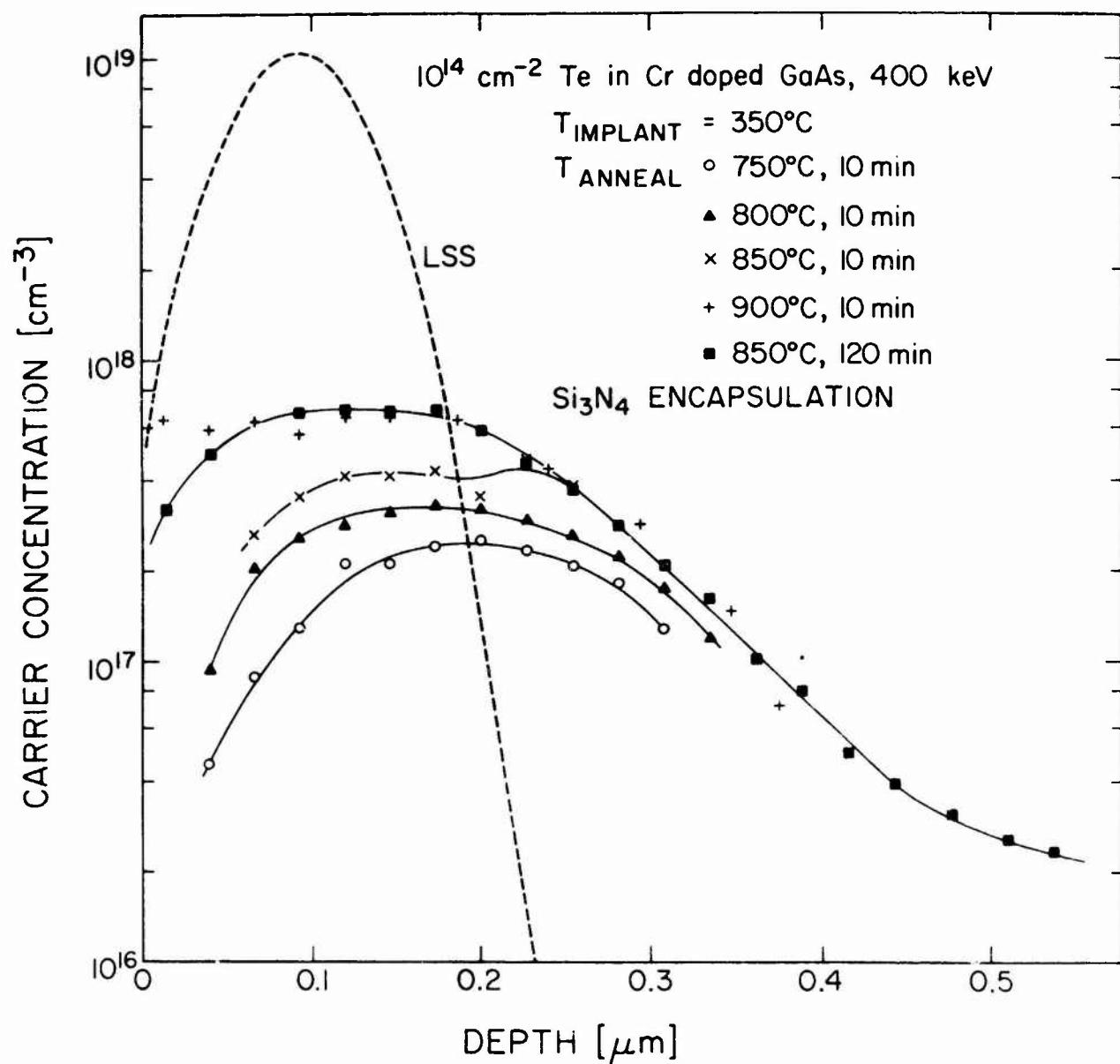
Fig. 3.3-2 Electron concentration profiles for semi-insulating GaAs samples implanted with 400 keV tellurium ions at 350° to a dose of $10^{14}/cm^2$ and annealed at the indicated temperatures.

implantation doping results. It is possible that these apparent deep pro-
files are caused by some problem with the measuring technique or that they
may be due to changes in the semi-insulating substrate materials. If we
consider the portion of the profile outside the LSS Gaussian range distribu-
tion, excluding the very deep penetration, it can be seen from Fig. 3.3-2
that variations of the annealing temperature between 750° and 900° produces
only a small change in the depth of the doping profile. This indicates that
the tail in this region is not due to normal diffusion processes. These
would be expected to produce much larger differences with anneal temperature
than are observed.

Several implantations have been carried out in which the sample was care-
fully aligned using the backscattering of helium ions to determine the align-
ment relative to the incident beam. Implantations were carried out with the
tellurium beam parallel to the (110) planes of the sample, or carried out in
a carefully-chosen random direction. The results of these experiments are
shown in Fig. 3.3-3. Data are available for only one randomly-implanted
sample. The difference between the results for the two planar-channeled
implants may be due to the fact that the caps were deposited at different times.
The results in Fig. 3.3-3 suggest that at least a portion of the doping tail
may be produced by planar channeling. The implants are normally carried out
in an orientation such that the (100) axis of the sample is oriented approxi-
mately 10° away from the incident beam direction. However, the orientation
in which the samples are mounted makes it likely that the beam is incident
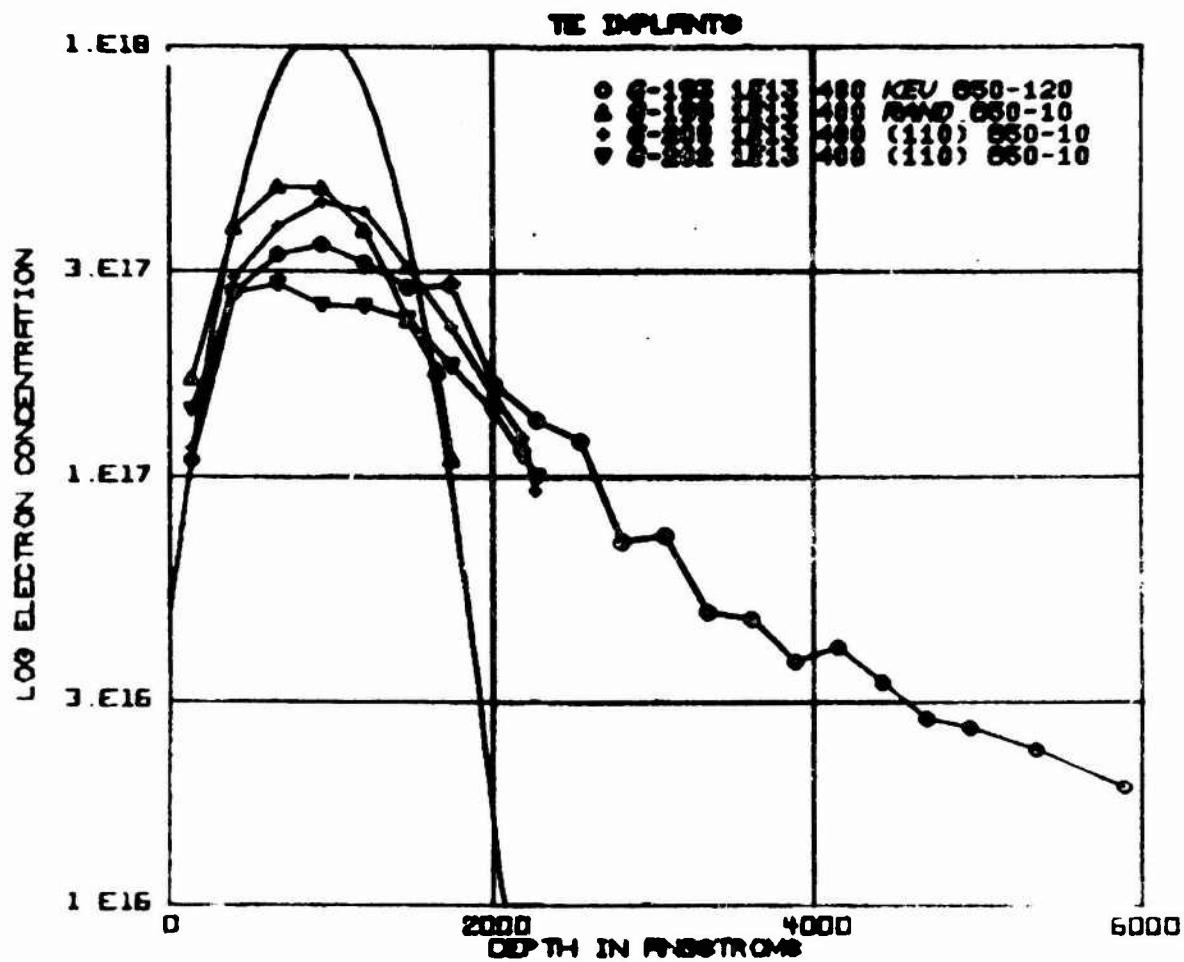
Fig. 3.3-3 Electron concentration profiles for samples implanted with 400 keV tellurium ions at 350° to a dose of 10^{13}/cm² with the samples aligned by helium ion backscattering so the tellurium ions penetrate either in a random direction or parallel to {110} planes. The samples were annealed at 850° for 10 minutes.

in a direction close to parallelism with the (110) planes. Because of the limited nature of the data comparing random and channeled orientations, we feel it is necessary to do further experiments before the contribution of channeling to the doping tail can be firmly established. However, it seems unlikely that planar channeling can account for the very deeply penetrating tails which have been observed in only a few samples.

Mobility profiles for the samples represented in Figs. 3.3-1 and 3.3-2 are presented in Figs. 3.3-4 and 3.3-5. The data in Fig. 3.3-4 for samples implanted with a dose of 10^{13} Te ions/cm^2 shows a trend of increasing mobility with increasing anneal temperature. In contrast to this, the data for the samples implanted with a dose of 10^{14} Te ions/cm^2 shown in Fig. 3.3-5 indicates that the mobility is approximately the same at a given depth irrespective of the annealing temperature. The dashed curves in these two figures are the values of mobility expected in good epitaxial samples of GaAs[25] with carrier concentrations at any particular depth equal to those observed for the samples annealed at 850° for 120 minutes. At depths of approximately 1000Å, the difference between these dashed curves and the profiles observed in the implanted samples is much greater for the samples implanted with doses of 10^{14}/cm^2 than for those implanted with doses of 10^{13}/cm^2. This difference and the lack of dependence of the mobility on annealing temperature suggests that a large density of scattering centers is present in the implanted layer, and that these scattering centers are not removed by annealing temperatures as high as 900° for periods of 10 minutes. Such scattering centers might be due
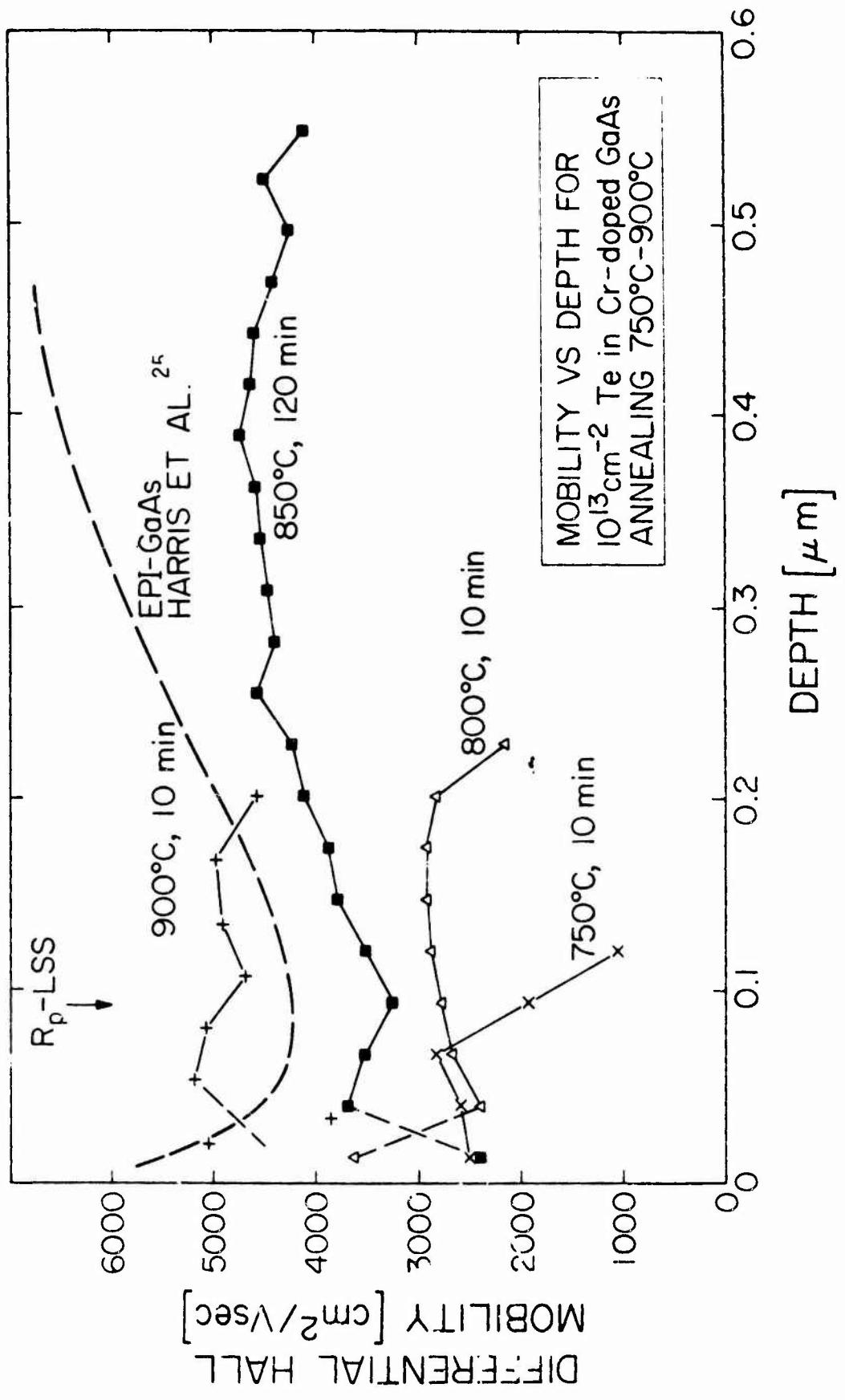
Fig. 3.3-4 Mobility profiles for the samples of Fig. 3.3-1.
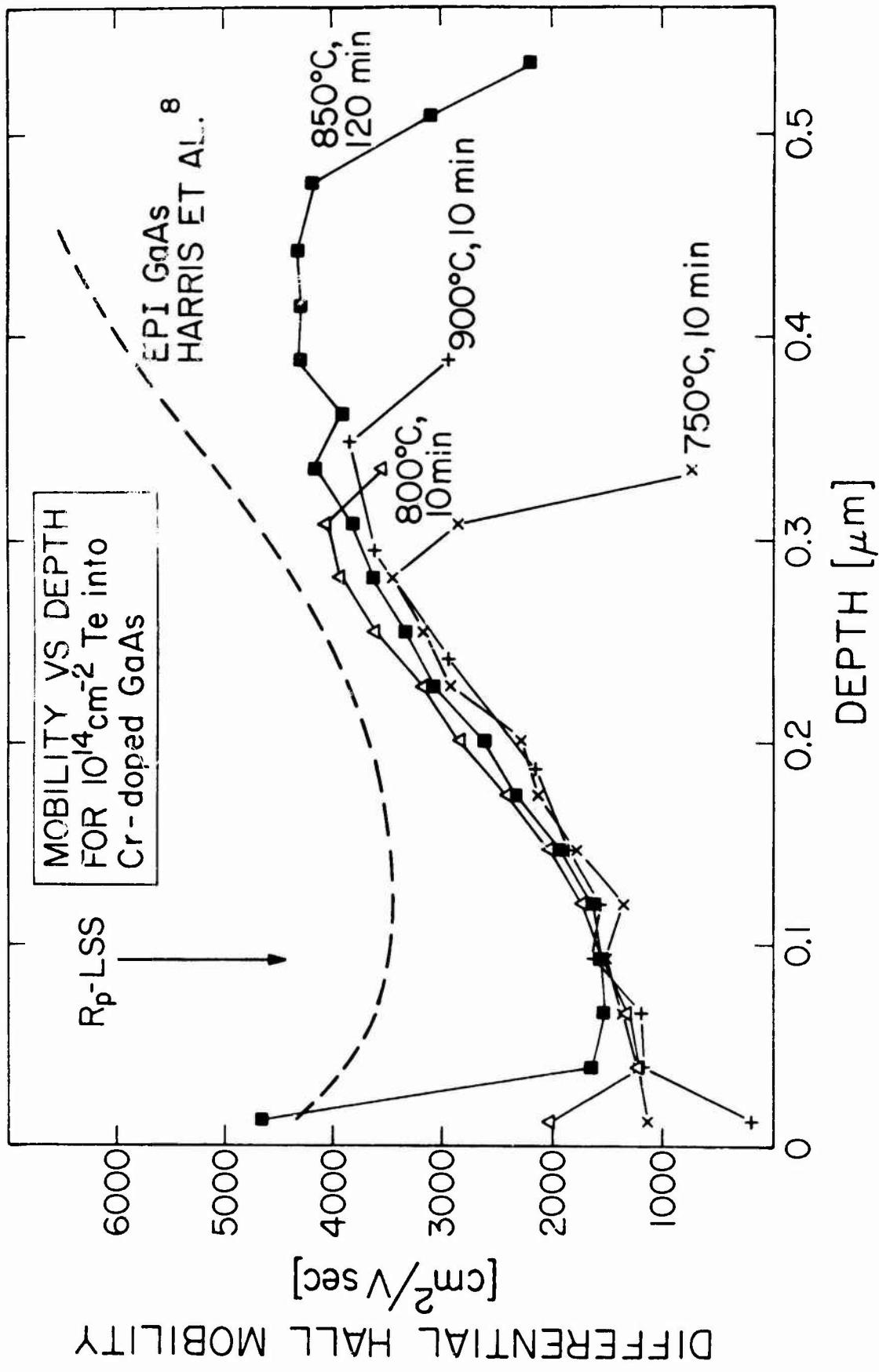
Fig. 3.3-5 Mobility profiles for the samples of Fig. 3.3-2.

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to incomplete annealing of the disorder introduced during implantation, or
may involve the implanted tellurium in some way.

The scattering centers which cause the lower mobility may also act as
compensating centers resulting in the low activation of the implanted
tellurium. A further indication of the presence of such centers is shown
in Fig. 3.3-6, which presents a comparison of electron concentration pro-
files measured in samples implanted with doses of 10^{13}, 10^{14}, or 10^{15} Te
ions/cm^2 and annealed at 900° for a period of 10 minutes. The data for the
sample implanted with a dose of 10^{15} Te ions/cm^2 shows that the carrier con-
centration in that sample is lower than in the sample with the 10^{13} dose to
depths of nearly 1500Å and lower than the concentration in the sample with
the 10^{14} dose to depths beyond 2000Å. Since earlier backscattering data for
GaAs samples implanted with doses of about 10^{15} Te ions/cm^2 and annealed
with Si_3N_4 caps indicates that there is little, if any, outdiffusion of the
implanted tellurium or spreading of the tellurium profile,[26] it seems that
some form of compensating center must be involved in producing this low
electron concentration near the surface of heavily-implanted samples. We
shall return to a discussion of this point later in this section.

Several experiments have been carried out in an effort to determine the
extent to which the substrate materials may affect the results of implantation
doping of GaAs. Figure 3.3-7 shows a comparison of electron concentration and
mobility profiles obtained from a Cr-doped semi-insulating substrate and from
an n-type epitaxial substrate of GaAs implanted with doses of 10^{14} 400 keV
Te ions/cm^2. Both the electron concentration profile and the mobility profile
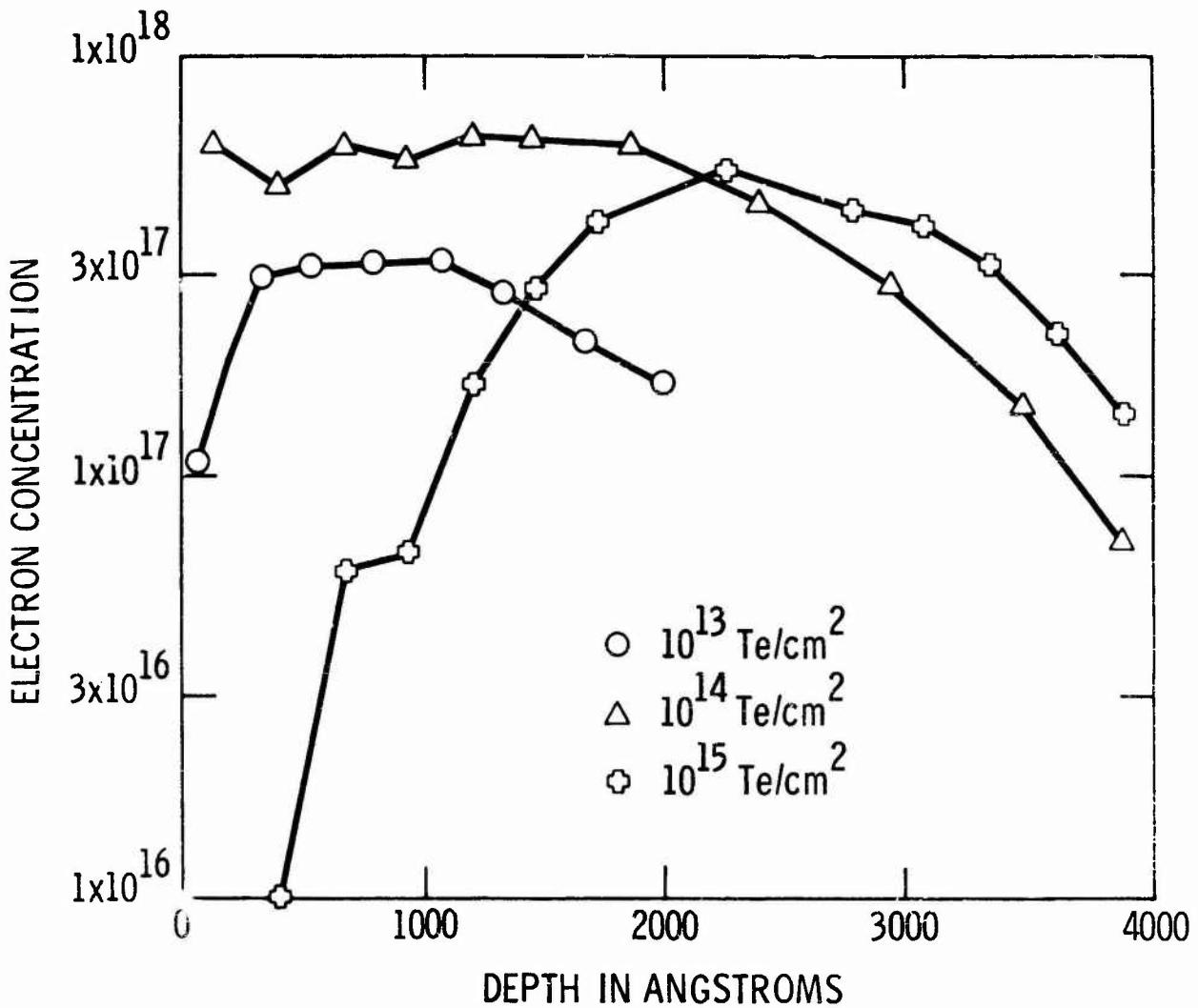
Fig. 3.3-6 Electron concentration profiles for samples of semi-insulating GaAs implanted with the indicated doses of 400 keV tellurium ions and annealed at 900° for 10 minutes.
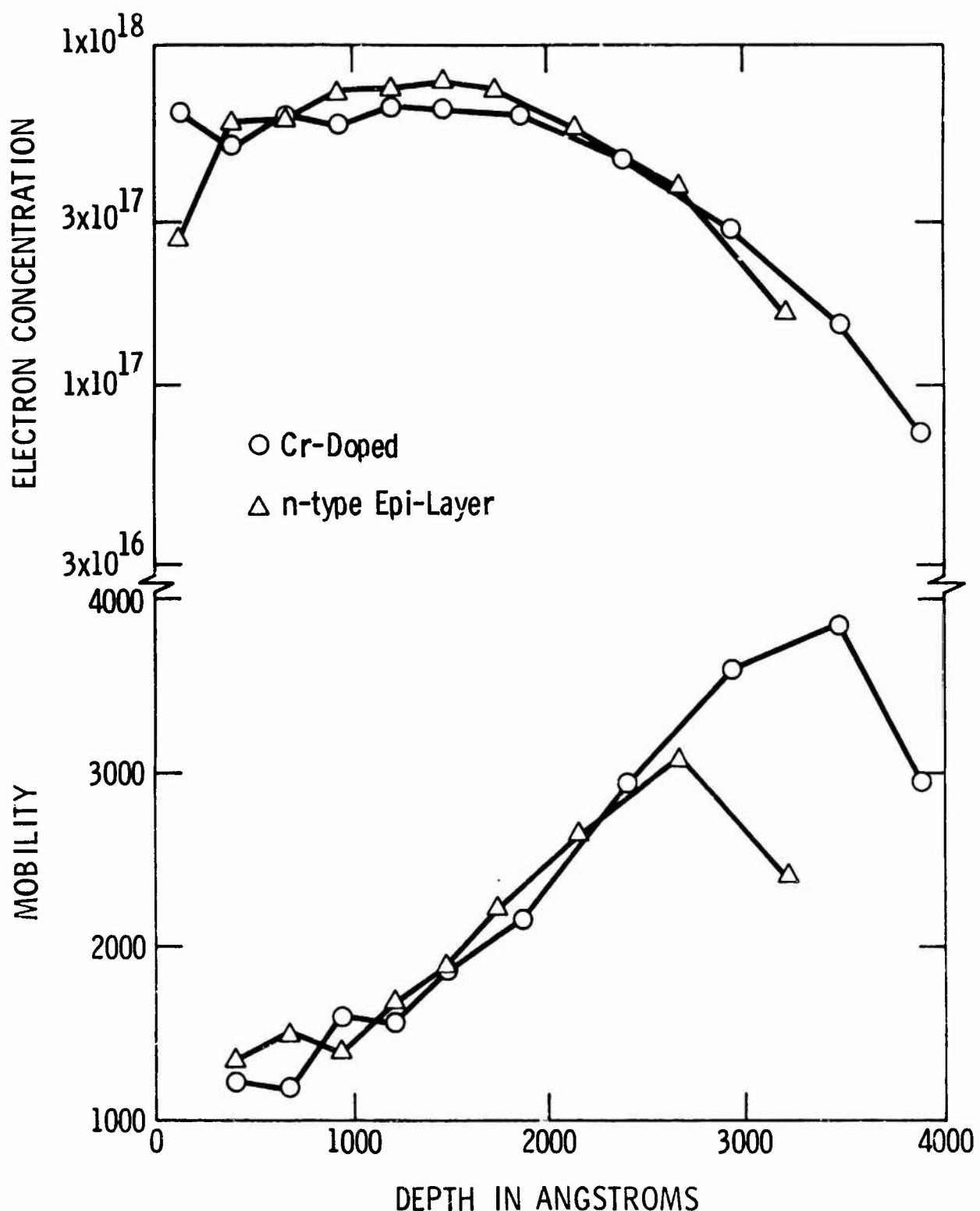
Fig. 3.3-7 Comparison of electron concentration and mobility profiles in a semi-insulating GaAs sample and an n-type epitaxial GaAs sample implanted with 400 keV tellurium ions at 350°. The dose was 10^{14} ions/cm^2, and the samples were annealed at 900° for 10 minutes.

for these two samples are very similar. A comparison of profile results for
implantation doses of 10^{14} Te ions/cm^2 in Cr-doped semi-insulating materials
obtained from two different suppliers is shown in Fig. 3.3-8. Again, the
results obtained in these two different implantation substrates are nearly
identical. In another experiment of this type, semi-insulating material from
four different suppliers was implanted with doses of 10^{13} Te ions/cm^2. The
samples were annealed at 850°C for a period of 30 minutes. The mobility and
electron concentration profile results are presented in Fig. 3.3-9. The
interpretation of these results may be complicated somewhat by the behavior
of the Si_3N_4 annealing cap on individual samples during annealing. The nitride
cap was deposited on all samples at the same time; and, therefore, would be
expected to have the same properties. It was observed that there was some
bubbling of the cap on the Bell & Howell samples, and that the cap had lost
contact with the surface on the MRC and Crystal Specialties samples following
annealing. The cap on these two samples did not rupture. However, pitting
of the surface, which was apparent following removal of the cap, indicates that
there was some loss of material from the surface. The reasons for this differ-
ent behavior of the nitride on these samples are not clear at present. Some
of the same material has been employed in subsequent implantation experiments
in which no lifting or bubbling of the nitride was observed. Possibly, the
differences between samples may be connected with surface contamination of
some samples following the routine etching procedure which is employed in pre-
paring samples for implantation. The data in Fig. 3.3-9 indicate that there

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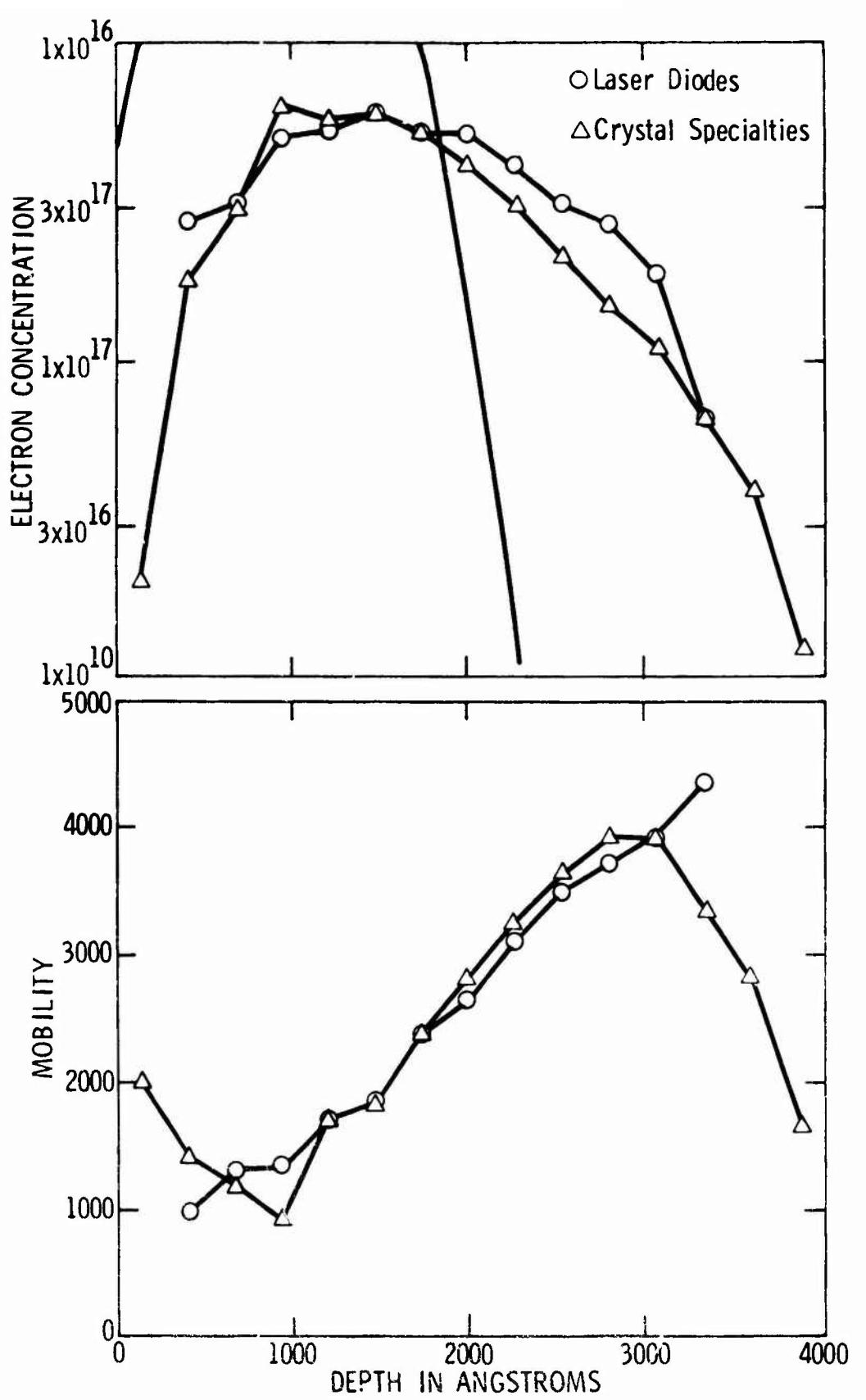
Fig. 3.3-8 Comparison of electron concentration and mobility profiles
in semi-insulating GaAs samples from two different
suppliers implanted with 400 keV tellurium ions at 350°.
The dose was 10^{14} ions/cm² and the samples were annealed
at 850° for 30 minutes.
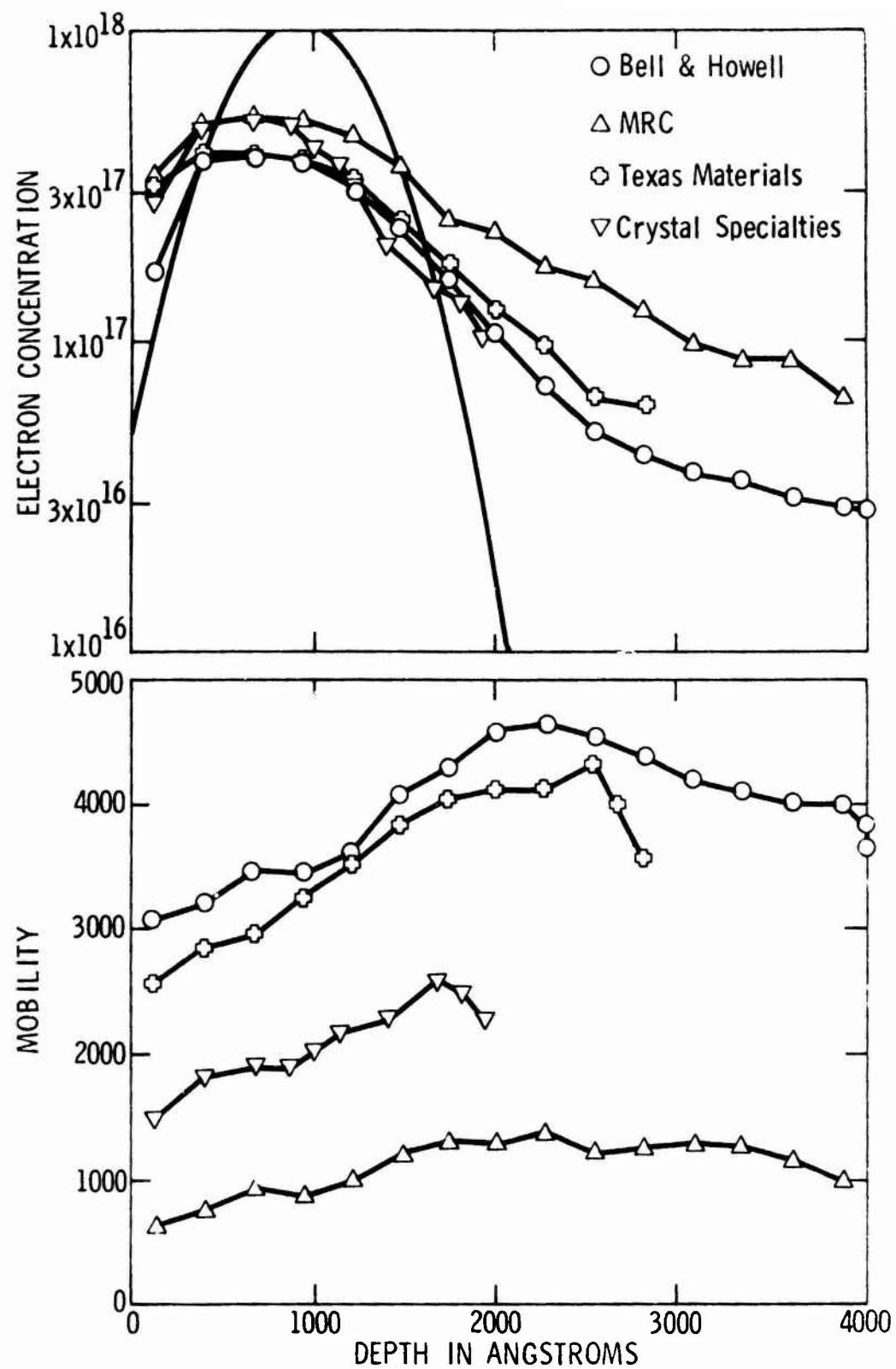
Fig. 3.3-9 Comparison of electron concentration and mobility profiles for semi-insulating GaAs samples from four different suppliers implanted with 400 keV tellurium ions at 350°. The dose was 10^{13} ions/cm² and the samples were annealed at 850° for 10 minutes.

is only a small difference in the carrier concentration achieved in the region of the maximum carrier concentration, but that the differences between different sample materials become larger in the tail region of the profile. Substantial differences in the mobilities obtained in the different samples are shown. The reasons for these differences are not clear at present.

These experiments using different implantation substrates indicate that the maximum carrier concentration which can be achieved by tellurium ion implantation doping of GaAs is not strongly dependent on the substrate material. It may be, however, that the details of the profile in the tail region particularly whether or not a very deep tail is produced may depend upon the substrate material.

The implantation of a group VI dopant, which is expected to occupy positions on the arsenic sublattice of GaAs, into GaAs produces a non-stoichiometry in the implanted region. That is, after implantation, there is an excess of atoms which should occupy arsenic lattice sites or, therefore, a deficiency of gallium atoms. In an attempt to determine whether or not this gallium deficiency is important in limiting the maximum electron concentrations achieved by tellurium implantation, we have carried out experiments in which gallium was implanted either before or after the implantation of the tellurium dopant. All implantations were carried out at a temperature of 350°. Because a 100 keV accelerator was used to provide the gallium beam, the energy of the tellurium was limited to 160 keV in order to have approximately the same pro-

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jected ranges for the gallium and the tellurium. The electron concentration
profile results for three samples--one without a gallium implant, the others
with gallium implanted either before or after the tellurium--are shown in
Fig. 3.3-10. The LSS range predictions for tellurium and gallium within the
concentration range of the figure are also shown. It can be seen that the
electron concentration profiles are very similar and no significant effects
of the gallium implantation are apparent. The mobility profiles have not
been shown in a figure, but they are also nearly identical.

Several tellurium implantations have been carried out using currents
approximately one-tenth that normally employed in performing implantations
with a dose of 10^{14} ions/cm^2. Results from two of these samples, compared
with the results from the sample using the normal tellurium current, are
shown in Fig. 3.3-11. The low current samples show a higher peak electron
concentration. This is, in fact, the highest electron concentration observed
for tellurium doping during the recent work on this contract. The results
are again somewhat clouded by the fact that for these two low-current implants
there was some lifting of the nitride without rupturing during annealing.
Some limited pitting of the surface was apparent following removal of the
nitride. At this point, it is not clear whether or not this lifting is
important in obtaining the higher electron concentration results observed
for these low-current implants. The results, however, suggest the possibility
that a limited loss of arsenic from the sample may be beneficial in that it
would tend to compensate for the non-stoichiometry produced by implantations,
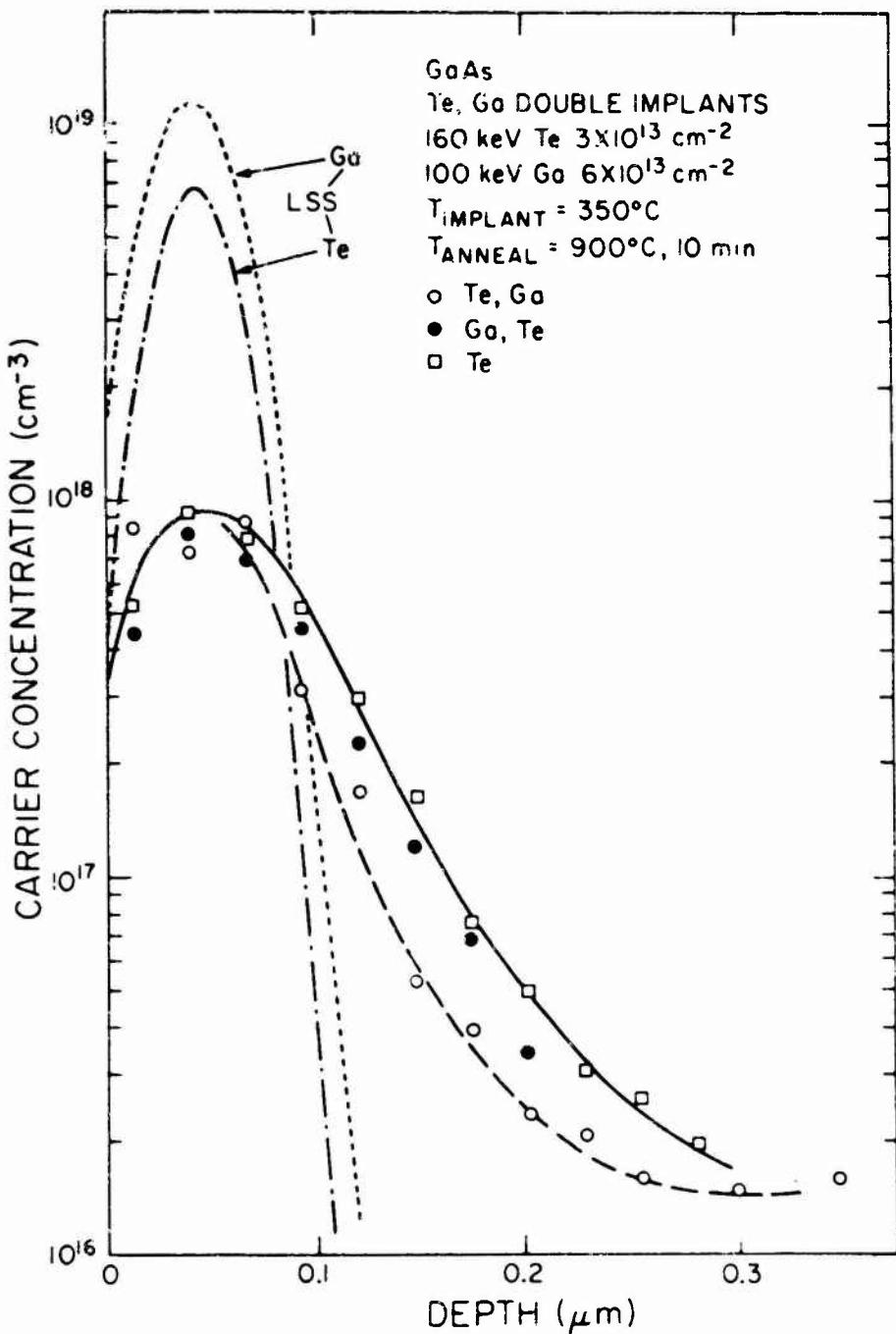
Fig. 3.3-10 Electron concentration profiles for semi-insulating GaAs samples implanted with tellurium and gallium as indicated. The doses used and the order of tellurium and gallium implantation are as noted in the inset. Implantations were carried out at 350°, the tellurium energy was 160 keV and the gallium energy was 100 keV. The samples were annealed at 900° for 10 minutes.
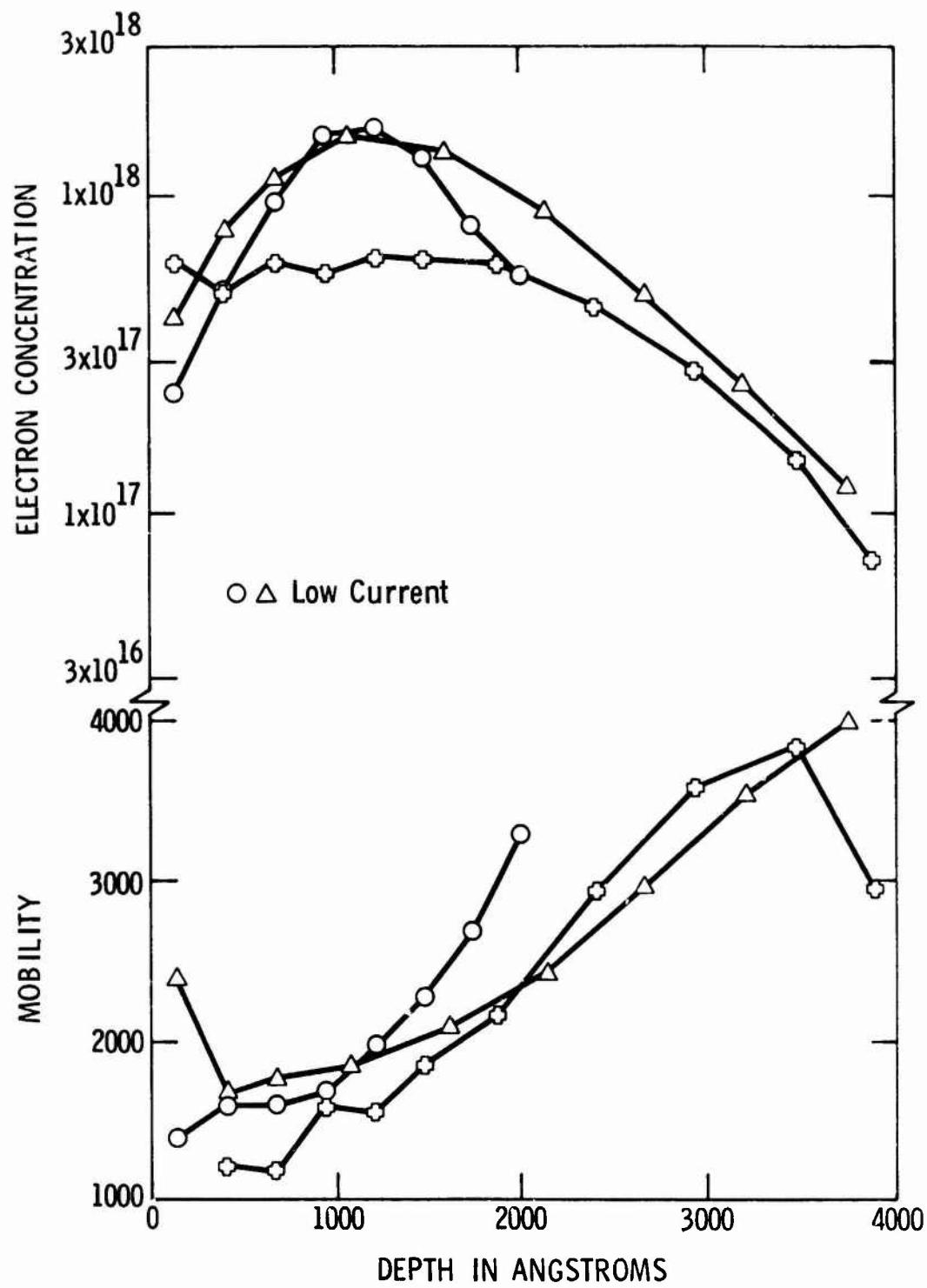
Fig. 3.3-11 Comparison of results for two low-current, 400 keV tellurium implants and one performed at the usual higher current, all at 350°. The dose was 10^{14} ions/cm^2 and the samples were annealed at 900° for 10 minutes.

discussed in the preceding paragraph. This point will be discussed further below, and experiments to investigate it suggested. It should be noted that in addition to higher electron concentrations, the low-current-implanted samples also display slightly higher electron mobilities in the region of the high concentration.

Data comparing implantation of 160 keV tellurium ions at either 150°C or 350°C are shown in Figs. 3.3-12 and 3.3-13. While the higher implantation temperature yields an electron concentration profile which is slightly higher than that obtained for the implantation carried out at 150°C, the mobility results are higher for the implantation performed at 150°C. The differences, however, are small and considering the limited nature of the data, it does not seem possible to decide at this time whether or not variation of the implantation temperature over the range studied will have a significant effect on the resulting doping profiles.

Preliminary experiments on selenium implantation doping have been carried out. The implantation energy was 100 kV. Doses of 5×10^{12} and 5×10^{13} Se ions/cm^2 have been employed at temperatures of 350°C during implantation. Profiles for these two doses are shown in Fig. 3.3-14. The peak concentration observed for the higher dose is about $2\times10^{18}/cm^3$. While further work must be done to determine the repeatability of this result, it is encouraging to have achieved as high an electron concentration as this in the first attempt with selenium doping. The results suggest that it may be profitable to explore selenium doping further as a means of producing highly-doped contact regions in GaAs.
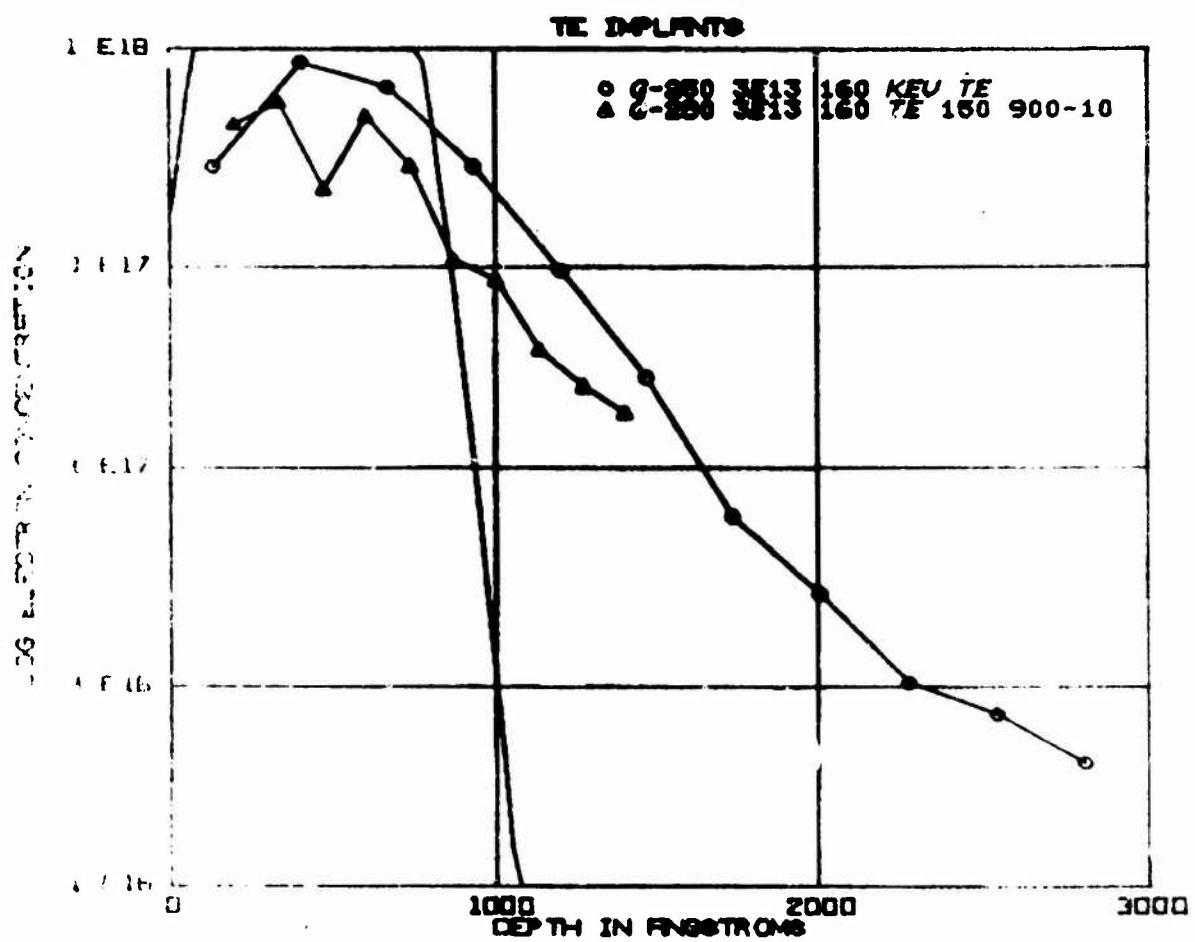
Fig. 3.3-12 Comparison of electron concentration profiles for
semi-insulating GaAs samples implanted with 160
keV tellurium ions at 150° (Δ) and at 350° (O).
The dose was 3×10^{13} ions/cm^2 and the samples were
annealed at 900° for 10 minutes.

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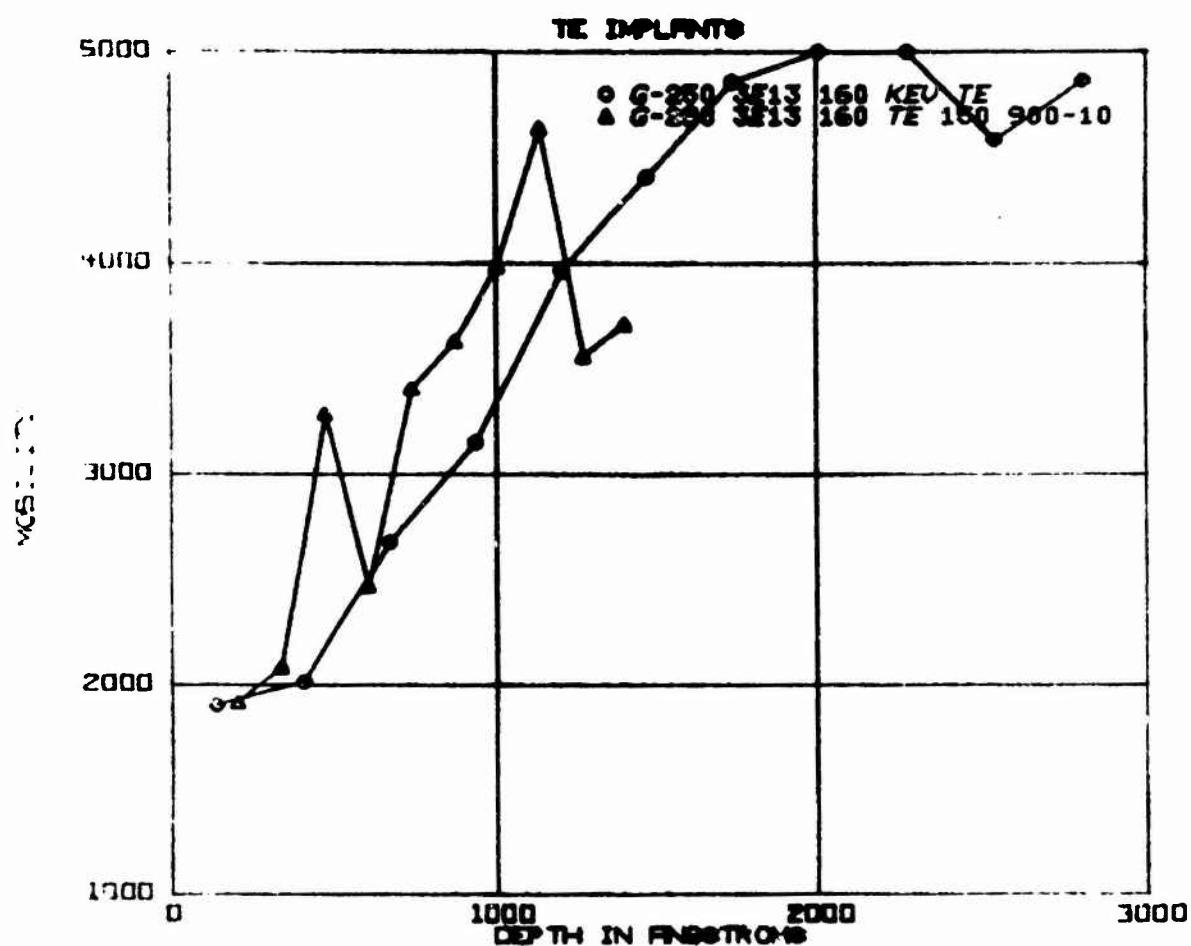
Fig. 3.3-13 Mobility profiles for the samples in Fig. 3.3-12.
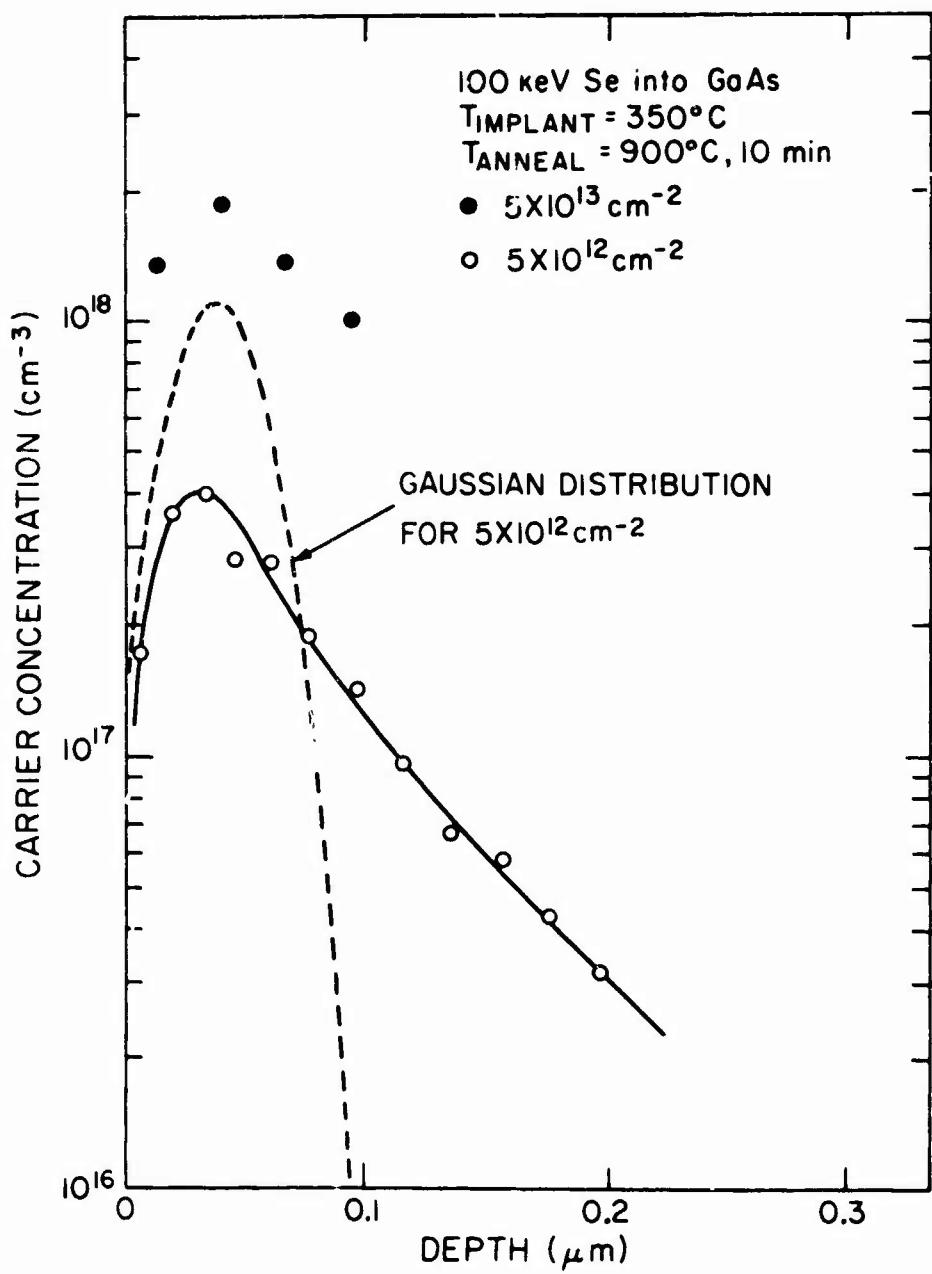
Fig. 3.3-14   Electron concentration profiles for semi-insulating
GaAs samples implanted with 100 keV selenium ions
at 350°.   Doses of 5×10^{12} (O) and 5×10^{13} (●)
ions/cm^2 were used and the samples were annealed at
900° for 10 minutes.

Electron concentrations achieved by tellurium doping in the present work are lower than those which were observed in some cases in the past. Except for the data in Fig. 3.3-11 the maximum electron concentrations achieved are about $7-8\times10^{17}/cm^3$. The results in the first scientific report[27] included one case in which a carrier concentration approximately 10 times as high was reported for implantation into a p-type substrate which was annealed with an A&N cap. The reason for the lower maximum concentrations in the present work is not clear at present. There are several cases in the literature in which tellurium doping in melt-grown crystals as high as 5 or $6\times10^{18}/cm^3$ is reported.[28,29] Therefore, it seems that the maximum concentration observed in most of our implanted samples is well below the intrinsic limit on tellurium doping. It is known, however, that the annealing of melt-grown crystals doped with tellurium reduces the electron concentration, with the concentration becoming lower at lower annealing temperatures. It has been reported that gallium-vacancy-tellurium-complexes are formed during this annealing, and the observed reduction in electron concentration is thought to be due to the compensation produced by these acceptor centers.[30] Since the implantation of tellurium in the GaAs produces a gallium deficiency, it is tempting to conclude that the formation of gallium-vacancy-tellurium-complexes may be more favorable in the implantation doping case, and that this may account, at least in part, for the low maximum carrier concentrations observed. If this is so, then any change in conditions during implantation or annealing which tends to correct

the non-stoichiometry produced during implantation might be expected to result in higher electron concentrations. The experiments in which gallium was implanted as well as tellurium have so far yielded negative results. At this point, these results cannot be regarded as conclusive evidence that gallium-vacancy-tellurium-complexes are not a dominant factor in determining the maximum electron concentration. The experiments have been quite limited in number, and it may be, for example, that the proper conditions for the gallium implantation have not yet been achieved. In addition to implanting gallium, it also seems reasonable to consider the possibility that the loss of a limited amount of arsenic from the sample during annealing might also tend to correct the non-stoichiometry produced during implantation. In fact, the results presented in Fig. 3.3-11, where higher than usual maximum carrier concentrations were achieved and some lifting of the nitride was observed, may indicate that a controlled arsenic loss would be beneficial. A simple experiment for checking this point would be to subject samples to annealing in the temperature range of about 600 to 700°C before they are capped with Si_3N_4 and annealed to still higher temperatures. The possibility that some of the compensating and scattering centers mentioned earlier in connection with the discussion of Figs. 3.3-1 through 3.3-5 may be due to unannealed damage effects should also be considered. Experiments to observe the annealing of ion bombardment damage in fairly-heavily-doped GaAs samples may be in order. The fact that, as shown in Fig. 3.3-11, we have in some cases achieved electron concentrations significantly higher than those observed in

most of the work, indicates that we have not as yet found the best conditions
for obtaining high doping in tellurium implantations in GaAs. It should be
noted, however, that for high implantation doses, 100% activity is unlikely
since even in doping of melt-grown or epitaxial GaAs by tellurium or selenium
an electron concentration less than the concentration of the dopant is
observed at dopant concentrations above about $4\times10^{17}/cm^3$.[29]

4.0 FUTURE PLANS

4.1 Epitaxial Growth and Material Characterization

4.1.1 High-Resistivity GaAs Layers

The following areas of investigation are planned at Stanford
University:

1. The effects of growth conditions on the incorporation of
   residual impurities, chromium, and oxygen in the SiO_2-BN-H_2
   system will be studied after replacing the graphite cradle
   with a fused quartz cradle to eliminate reactions involving
   carbon.

2. The minority carrier diffusion lengths in the epitaxial
   layers will be measured using scanning electron microscope
   techniques.

3. Electron transport mechanisms will be studied.

4.1.2 Material Characterization

4.1.2.1 IMPATT Diode Analysis and Measurements. Further studies
of the electronic quality factor will be carried out to gain

better information about material parameters and how they

affect distortion properties and bandwidth of IMPATT amplifiers.

In particular, more measurements of IMPATT amplifiers utilizing

flat doping as well as Read-type structures will be made to obtain

further information about material parameters in GaAs like the

effective avalanche width. Low-frequency noise measurments will

be initiated to determine the intrinsic response time.

4.1.2.2 <u>Annealing Study</u>. The progress in this study has produced

$p\nu n^+$ structures with good breakdown characteristics. Such struc-

tures will be used in multiplication measurements to determine

ionization rates in GaAs.

4.2 Semi-Insulating Material

Some more in depth work on the p-i-p and n-i-n structures will be done

and simplification of the sample construction and measurement technique will

be sought. The effect of varying growth conditions will be studied in order

to test the compensation mechanism, to test how sensitive the quality of the

material is to growth conditions, and to improve the quality of the materials.

A systematic study will be carried out on the possibility that impurity

diffusion may explain the apparent junction location in the measured p-i-p

and n-i-n structures.

4.3 Ion Implantation

Experiments designed to give information on the reasons for the low maxi-

mum electron concentrations generally achieved by tellurium implantation will

be carried out. These include experiments in which the implanted sample will

be annealed to temperatures of the order of 600 to 700°C in a hydrogen atmosphere

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in an effort to produce a limited loss of arsenic from the surface. Following
this they will be capped and annealed to a temperature of 900°C. Gallium
implantation and ion damage experiments may also be pursued. Selenium
implantation doping will be explored in more detail to see if the preliminary
encouraging results are reproducible. Considerable emphasis will also be
placed upon exploring techniques for producing lower electron concentrations
with doping profiles suitable for the channel regions of FET devices. This
will initially involve a study of sulfur implantation including the effects
of varying doses and anneal temperatures on the electron concentration pro-
files produced. It is also anticipated that sulfur tracer experiments will
be carried out in an effort to determine the spatial location of the sulfur
which did not contribute to the electron concentration profile and to gain
information on the mechanisms responsible for the deep doping observed in
sulfur implantation.

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